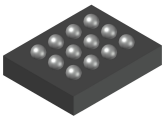
25 V/5 A Rated OVP with Low On-resistance and Integrated TVS

FPF3382UCX



WLCSP12
CASE 568AP

General Description

FPF3382 is an Over-Voltage Protection device with integrated low on-resistance single channel switch and TVS.

The device contains an N-MOSFET that can operate from 2.8 V to 25 V and can support a maximum continuous current of 5 A. When the input voltage exceeds the over-voltage threshold, the internal FET is turned off immediately to prevent damage to the protected downstream components. The device has integrated ±110 V surge protection TVS based on IEC61000-4-5 standards.

FPF3382 is available in a small 12-bump WLCSP package and operate at the temperature range of −40 °C to +85 °C.

Features

- Internal Low Rdson NMOS Transistors: Typ. 13 mΩ
- Current Capability: Maximum Continuous Current 5 A
- Up to +28 V Input Voltage ABS
- Fast OVP Response Time: Typical 40 ns
- Externally Adjustable OVP with OVLO Pin
- Active Low Enable Control Pin: CTRL
- VDET can Souring 1 mA MIN Current Output
- Surge Integrated TVS, IEC61000-4-5: ±110 V
- Over Temperature Protection (Thermal Shutdown)
- Support System Level ESD Based on IEC61000-4-2:
  - Contact Discharge: ±10 kV
  - Air Gap Discharge: ±15 kV
- Electrostatic Discharge Capability (ESD):
  - Human Body Model (HBM): ±2 kV
  - Charged Device Model (CDM): ±1 kV
- Hot Plug can Support +28 V
- This Device Pb-Free, Halide Free and is RoHS Compliant

Typical Applications

- Smart Phones, PDA and PGS
- Tablets, Netbooks, Ultra-Mobile PCs
- Gaming Devices and E-books

MARKING DIAGRAM

3S	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
U	= Wafer Number Code
ZZ	= Assembly Lot Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

Application Diagram

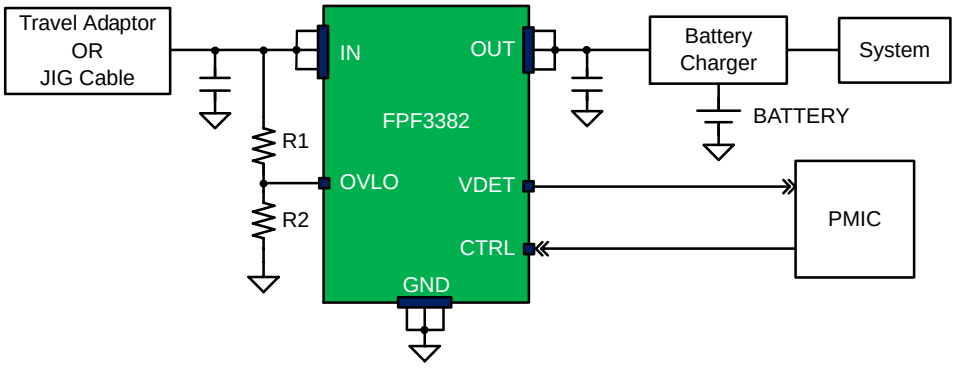


Figure 1. Typical Application

Block Diagram

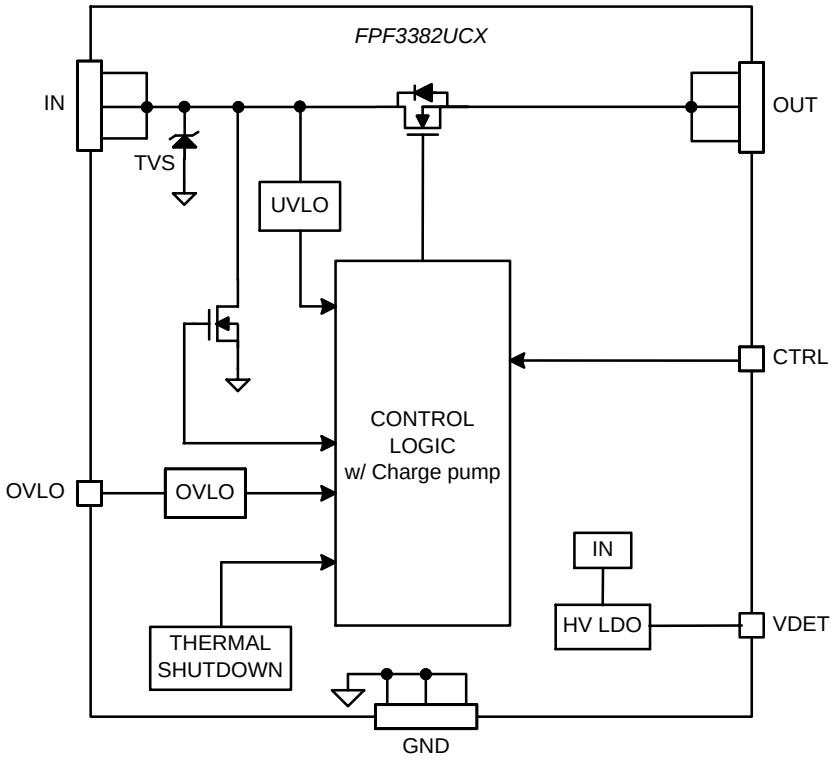


Figure 2. Simplified Block Diagram

Pin Configuration

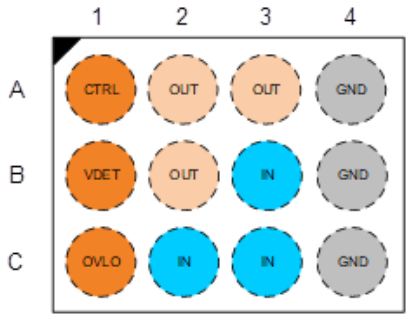


Figure 3. Pin Configuration (Top View)

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Type	Description
A4, B4, C4	GND		Ground
C1	OVLO	OVLO Input	Over Voltage Lockout Adjustment Input
B3, C2, C3	IN	Power Input	Power FET Input and Device Supply
A2, A3, B2	OUT	Power Output	Power FET Output
B1	VDET	Power Output	Regulated Output according to IN
A1	CTRL	Enable Input	Active Low with internal 1 MΩ pull down resistor

MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{IN}	Input Voltage Range		−0.3	28	V
V_{OUT}	Output Voltage Range		−0.3	V_{IN} + 0.3	V
V_{OVLO}	Maximum DC Voltage Allowed on OVLO		−0.3	24	V
$V_{I/O}$	Maximum DC Voltage Allowed on CTRL and VDET to GND		−0.3	6.25	V
I_{OUT}	Internal FET Continuous Current		−	6.25	A
I_{PEAK}	Internal FET Peak Current (Pulse Width No Longer than 100 μs)		−	7	A
t_{PD}	Total Power Dissipation at T_A = 25 °C		−	1.48	W
T_{STG}	Storage Junction Temperature		−65	+150	°C
T_J	Maximum Junction Temperature		−	+150	°C
T_{SLD}	Lead Temperature (Soldering, 10 Seconds)		−	+260	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient (2S2P. 1 in. (Note 1) Pad of 2 oz. Copper)		−	84.1	°C/W
ΔPD/ΔT	Derating Factor Above T_A = 25 °C		−	−11.9	mW/°C
Surge	IEC61000-4-5 Surge		110	−	V
Hot Plug		Vbus rising up from 0 V with 6 V/μs slew rate; Ibus > 5 A	28	−	V
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI/ESDA/JEDEC JS-001	2	−	kV
		Charged Device Model, JESD22-C101	1	−	
	IEC61000-4-2 System Level (Note 1)	Air Discharge at VIN and VOUT	15	−	
		Contact Discharge at VIN and VOUT	10	−	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. External TVS is required.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	2.8	25	V
V_{OUT}	Output Voltage	2.8	V_{IN} + 0.3	V
V_{IO}	OVLO, CTRL and VDET	0	5.5	V
T_A	Ambient Operating Temperature	−40	85	°C
I_{OUT}	Output Current (Note 2)	−	5	A
I_{OTG}	OTG Current V_{OUT} to V_{IN}	−	1.6	A
C_{IN}	IN Capacitor	0.1	−	μF
C_{OUT}	OUT Capacitor	0.1	−	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
2. Life time, under maximum current, >5 years base on Temperature < 85 °C and no longer than 12 hours per day.

ELECTRICAL CHARACTERISTICS (V_{IN} = 2.8 to 25 V, C_{IN} = 0.1 μF, C_{OUT} = 0.1 μF, T_A = −40 to 85 °C; For typical values V_{IN} = 5.0 V, I_{IN} ≤ 3 A, C_{IN} = 0.1 μF, T_A = 25 °C, for min/max values T_A = −40 °C to 85 °C; unless otherwise noted.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
LEAKAGE AND QUIESCENT CURRENTS						
I_{IN}	Input Quiescent Current in Normal Operation	V_{IN} = 5 V, V_{OVLO} = 0.6 V, OUT floating, V_{CTRL} = 0 V	−	90	−	μA
		V_{IN} = 25 V, V_{OVLO} = 0.6 V, OUT floating, V_{CTRL} = 0 V	−	150	−	μA
I_{IN_OV}	Input current under Over Voltage Condition	V_{IN} = 25 V, V_{OVLO} = 1.8 V, OUT floating, V_{CTRL} = 0 V	−	150	−	μA
I_{OVLO}	OVLO Input Leakage Current	V_{OVLO} = V_{OVLO_TH}	−100	−	100	nA
OVER VOLTAGE AND UNDER VOLTAGE LOCKOUT AND I/O						
V_{IN_CLAMP}	Input Clamping Voltage during Surge (IEC61000-4-5) Event	I_{IN} = 30 A (Note 3)	−	37	−	V
		I_{IN} = 10 mA	−	32	−	V
$V_{IN\_UV\_R}$	Under Voltage Lockout Rising Trigger Level	V_{IN} Rising	−	2.5	2.6	V
$V_{IN\_UV\_F}$	Under Voltage Falling Trigger Level	V_{IN} Falling	−	2.35	−	V
V_{IN_OVLO}	Internal Over Voltage Trip Level	V_{IN} Rising, OVLO grounded	12.1	12.4	12.7	V
V_{OVLO_TH}	OVLO Set Threshold	V_{OVLO} = 1.1 V to 1.3 V, the voltage of OVLO pin to trigger Over Voltage condition	1.16	1.2	1.23	V
V_{HYS_OVLO}	OVLO Hysteresis		−	3	−	%
V_{OVLO_RNG}	Adjustable OVLO Threshold Range	V_{IN} Rising	4	−	25	V
$V_{OVLO\_SEL\_VIH}$	HIGH Threshold for Default OVLO	Voltage Increasing	0.2	−	−	V
$V_{OVLO\_SEL\_VIL}$	LOW Threshold for Default OVLO	Voltage Falling	−	−	0.1	V
V_{IH}	I/O Pin (CTRL) HIGH Voltage	CTRL Voltage increasing	0.84	−	−	V
V_{IL}	I/O Pin (CTRL) LOW Voltage	CTRL Voltage decreasing	−	−	0.54	V
RESISTANCE						
R_{ON}	On-resistance of Power Switch	V_{IN} = 5 V, I_{OUT} = 200 mA, T_A = 25 °C	−	13	20	mΩ
		V_{IN} = 25 V, I_{OUT} = 0.1 A to 5 A (Note 3)	−	13	20	
RPD	Pull-down Resistor on CTRL		−	1	−	MΩ
R_{IN_DISCH}	Discharging on IN (Optional)	V_{IN} = 5 V, V_{CTRL} = 1.8 V	−	550	−	Ω

ELECTRICAL CHARACTERISTICS (V_{IN} = 2.8 to 25 V, C_{IN} = 0.1 μF, C_{OUT} = 0.1 μF, T_A = −40 to 85 °C; For typical values V_{IN} = 5.0 V, I_{IN} ≤ 3 A, C_{IN} = 0.1 μF, T_A = 25 °C, for min/max values T_A = −40 °C to 85 °C; unless otherwise noted.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
TIMING CHARACTERISTICS						
t_{DEB}	De-bounce Time of Power Switch Turned On	Time from $V_{IN\ UV} < V_{IN} < V_{IN\_OVLO}$ to V_{OUT} = 0.1 x V_{IN}	−	15	−	ms
t_{ON}	Switch Turn-On Rising Time (Note 3)	V_{IN} = 5 V, R_L = 100 Ω, C_L = 1 μF, V_{OUT} from 0.1 x V_{IN} to 0.9 x V_{IN}	−	0.4	−	ms
t_{OFF}	Switch Turn-Off Time by CTRL (Note 3)	R_L = 10 Ω, C_L = 0 μF, $V_{CTRL} > V_{IH}$ to V_{OUT} = 0.9 x V_{IN}	−	−	2	μs
t_{OFF_RES}	OVP Response Time	R_L = 10 Ω, C_L = 0 F, time from $V_{IN} > V_{IN\_OVLO}$ to V_{OUT} = 0.9 x V_{IN}	−	40	−	ns
VDET						
V_{VDET_OUT}	VDET Clamp Voltage	V_{IN} = 5 V, I_{DET} = 0 mA, T_A = 25 °C	3.8	4	4.2	V
		V_{IN} = 25 V, I_{DET} = 0 mA, T_A = 25 °C				
		V_{IN} = 5 V, I_{DET} = 20 mA, T_A = 25 °C				
		V_{IN} = 25 V, I_{DET} = 20 mA, T_A = 25 °C				
I_{VDET}	VDET Current Capability		−	30	−	mA
V_{DET_SURGE}	VDET Surge	100 V surge on V_{IN} (IEC61000-4-5)	−	−	6	V
THERMAL SHUTDOWN (TSD)						
T_{SDN}	Trip Point	Thermal shut down threshold	−	130	−	°C
T_{SDN_HYS}	Hysteresis	Thermal shut down hysteresis	−	20	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design and characterization.
4. Depends on the capacitance on OVLO pin.

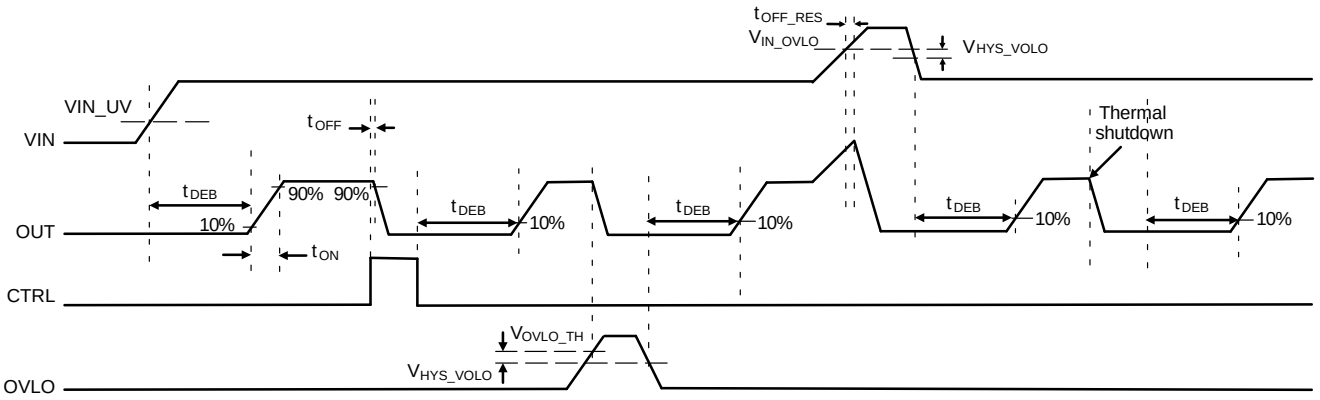


Figure 4. Timing for Power Up and Normal Operation

GENERAL

FPF3382 is an OVP power switch to protect next stage system which is optimized to lower voltage working condition. The device includes ultra-low on-resistance power FET (13 mΩ) and internal TVS for surge event protection based on IEC61000-4-5. The super-fast OVP response time is only 40 ns for default OVP condition.

Power MOSFET

The FPF3382 integrates an N-type MOSFET with 13 mΩ resistance. The power FET can work under 2.8 V~25 V and up to 5 A DC current capability.

Power Supply

The FPF3382 is supplied by IN. IN will be firstly supplied by OUT when the device is working under USB On-The-Go (OTG) condition.

Enable Control

FPF3382 has an active low enable pin CTRL. When CTRL pin is connected to a high level, the internal FET will be turned off. When CTRL pin is connected to low level, the FET will be turned on as long as VIN is not higher than Over-Voltage threshold.

Under Voltage Lockout

FPF3382 power switch will be turned off when the voltage on IN is lower than the UVLO threshold $V_{IN\_UV\_F}$. Whenever VIN voltage ramps up to higher than $V_{IN\ UV\_R}$. the power FET will be turned on automatically after t_{DEB} de-bounce time if there is no OV or OT condition.

Over Voltage Lockout

The power FET will be turned off whenever IN voltage higher than V_{IN_OVLO}. The value of V_{IN_OVLO} can be set by external resistor ladder or just be default value V_{IN_OVLO}. When V_{OVLO} is smaller than V_{IL_OVLO}, V_{OVLO} will be decided by default value. When V_{OVLO} is larger than V_{IH_OVLO}, the power switch will be turned off once $V_{OVLO} > V_{OVLO\_TH}$. The external resistor ladder can be decided according to the following equation:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times (1 + R1 / R2) \quad \text{(eq. 1)}$$

where R1 and R2 are the resistors in Figure 1.

Thermal Shutdown

When the device is in the switch mode, to protect the device from over temperature, the power switch will be turned off when the junction temperature exceeds TSD. The switch will be turned on again when temperature drop below $T_{SDN} - T_{SDN\_HYS}$.

VDET function

The FPF3382 provides a regulated voltage output on VDET according to IN. The voltage at VDET is not present while the FPF3382 is in thermal shutdown or IN is lower than the input operating range.

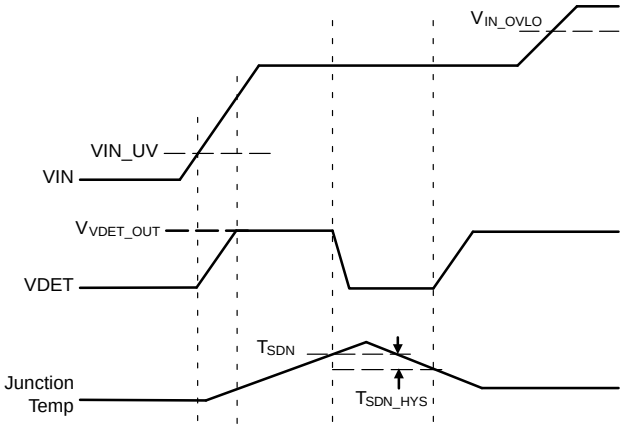


Figure 5. VDET Behavior

APPLICATION INFORMATION

Input Decoupling (Cin)

A ceramic or tantalum at least 0.1 μF capacitor is recommended. Higher capacitance and lower ESR will improve the overall line and load transient response.

Output Decoupling (Cout)

The FPF3382 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The minimum output decoupling value is 0.1 μF and can be augmented to fulfill stringent load transient requirements.

Thermal Considerations

As power in the FPF3382 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the FPF3382 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the FPF3382 can handle is given by:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad \text{(eq. 2)}$$

Since T_J is not recommended to exceed 125 °C, then the FPF332 soldered on 645 mm^2, 1 oz copper area, and the ambient temperature (T_A) is 25 °C. The power dissipated by the FP3382 can be calculated from the following equations.

$$P_D \approx V_{IN} \times \left(I_Q @ I_{OUT}\right) + I_{OUT}^2 \times R_{ON} \quad \text{(eq. 3)}$$

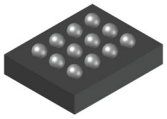
Hints

Vin and Vout printed circuit board traces should be as wide as possible. Place external components, especially the input capacitor and TVS, as close as possible to the FPF3382, and make traces as short as possible.

ORDERING INFORMATION

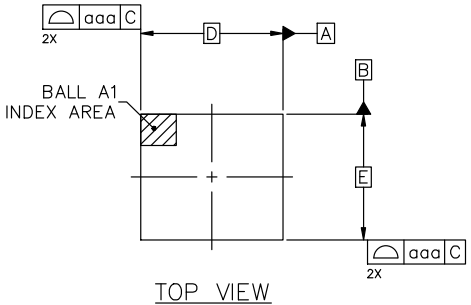
Device Order Number	Specific Device Marking	Package Type	Shipping†
FPF3382UCX	3S	WLCSP12 (Pb-Free, Halogen Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

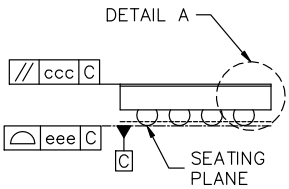


WLCSP12 1.76x1.56x0.32, 0.40P
CASE 568AP
ISSUE B

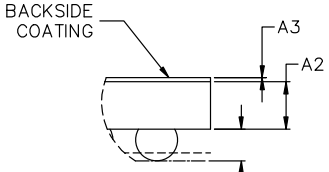
DATE 24 APR 2024



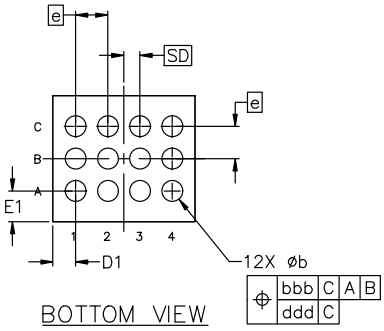
TOP VIEW



SIDE VIEW



DETAIL A'
SCALE 2:1

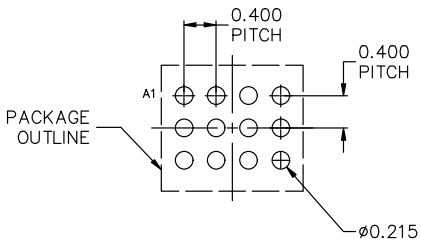


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

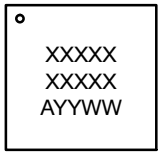
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.480	0.515	0.550
A1	0.176	0.196	0.216
A2	0.282	0.294	0.306
A3	0.022	0.025	0.028
b	0.250	0.265	0.280
D	1.760 BSC		
D1	0.265	0.280	0.295
E	1.560 BSC		
E1	0.365	0.380	0.395
e	0.400 BSC		
TOLERANCES OF FORM AND POSITION			
aaa	0.030		
bbb	0.050		
ccc	0.100		
ddd	0.030		
eee	0.050		



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON57157H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**WLCSP12 1.76x1.56x0.32, 0.40P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales