VE-Trac™ Direct Technical Guide

AND9987/D

This document is intended to be a guide to explain the technical details of the product features and capabilities. It is also designed to provide reference circuits and application related notes to ensure that the product is used in an optimal manner for its intended end use.

APPLIES TO THE FOLLOWING PARTS

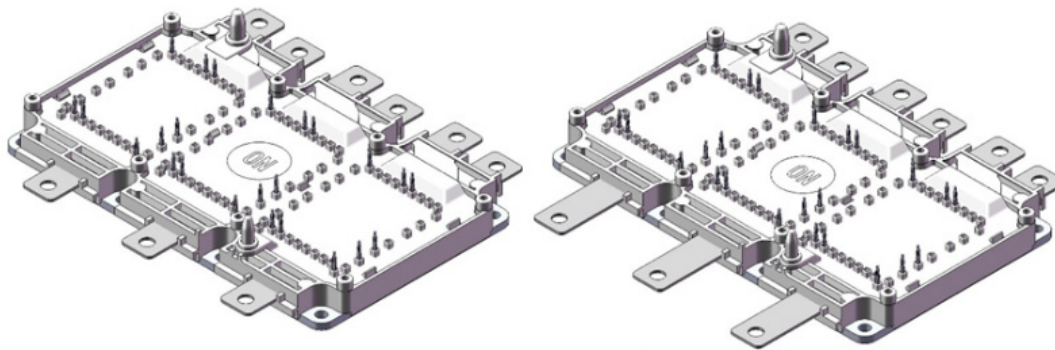|	
NVH820S75L4SPB	750 V, 820 A, Short Terminal
NVH820S75L4SPC	750 V, 820 A, Long Terminal

Figure 1.

INTRODUCTION

The VE−Trac Family of power modules is an automotive qualified line of products specifically designed for EV−traction inverters. The product line is broadly classified into two platforms (i) Dual (ii) Direct. Each platform has its own advantages, but this document's scope is limited to understanding the datasheet parameters and device characteristics of the Direct product line. It also includes a design guide and recommendations for using the product effectively. A separate document 'VE−Trac Direct Assembly Guide' provides details related to assembling the power module in an assembly.

VE−Trac Direct product features:
- Compatible with popular module footprint.

- Robust and reliable new press−fit pin design.
- More power compared to similar module package.
- Direct cooling with leading thermal performance.
- Continuous 150°C operation with limited operation at 175°C.
- Thermistor based temperature sense per phase leg.

TECHNICAL DETAILS

ON Semiconductor's latest generation of IGBTs and Diodes are incorporated into the VE−Trac products. The 750 V VE−Trac products use the latest 4th Generation of IGBTs from ON Semiconductor.
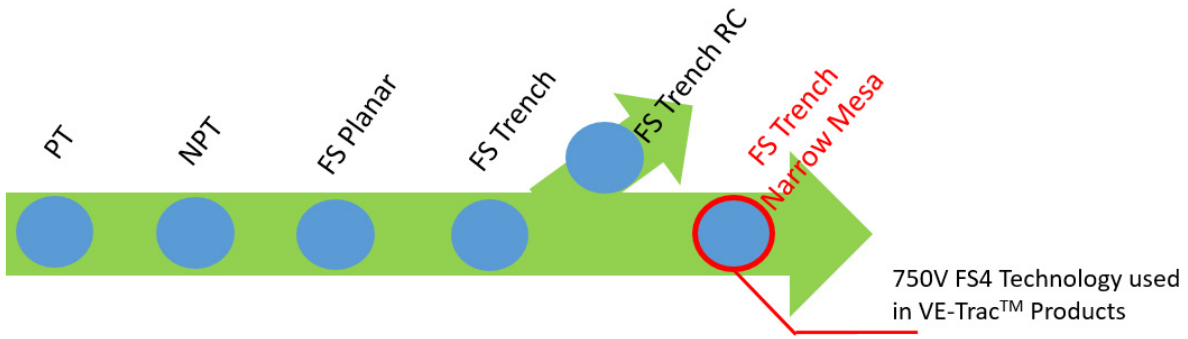
Chip Technology

Figure 2. ON Semiconductor Chip Technologies

This new generation of Field Stop (FS) IGBTs with a high density cell structure and an optimized double layer shows remarkable device performance under static and dynamic conditions with strong latch–up ruggedness. The design of the chip uses sub–micron trench and mesa active with a narrow mesa width.

Package Design

The VE–Trac Direct is a single side direct cooled package with a form factor that is now becoming more common for EV traction application. The package consists of power devices that are soldered to DBC and wire–bonded on the top side. The DBCs are attached to a copper base plate that has a pin–fin structure on the other side to enable direct cooling (see Figure 4).
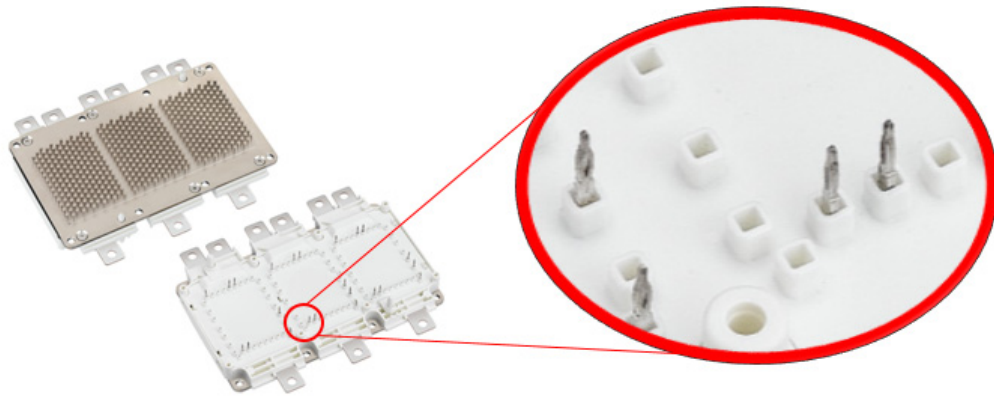

Figure 3. VE–Trac Direct Package Highlighting the Pin–fin Heatsink and Press–fit Pins

For the signal connections, the module includes press–fit pins that are designed to meet the stringent automotive standards. The press–fit pins are fixed in position and orientation as shown in Figure 3. Detailed information on mounting the module and gate driver board can found in the assembly guide.
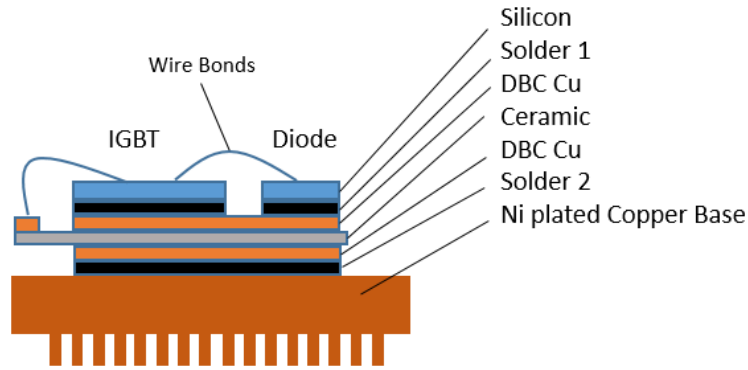
Figure 4. Illustrated Cross Section of the Package

The typical layout of the module is illustrated below with its pin assignments. Each phase leg has its DC power terminals on one side and the switching terminal on the opposing side with eight press−fit pins providing access to the signal terminals and the NTC thermistor located in each phase leg.
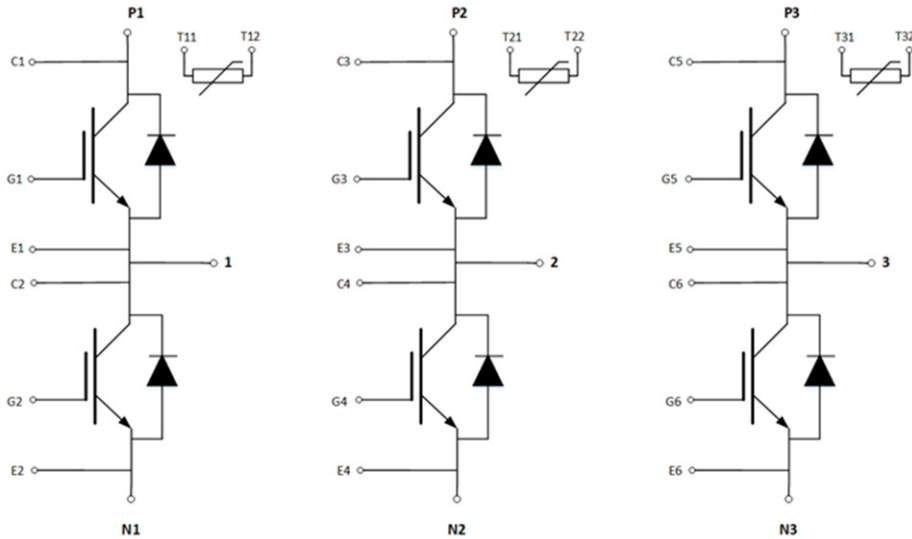

Figure 5. Schematic View of the 820 A, 750 V Version. Check the Data Sheet of Each Module Type to Verify the Information.

Table 1. EXAMPLE PIN ASSIGNMENT FOR 820 A, 750 V MODULE TYPE

Pin #	Pin Function Description
P1, P2, P3	Positive Power Terminals
N1, N2, N3	Negative Power Terminals
1	Phase 1 Output
2	Phase 2 Output
3	Phase 3 Output
G1–G6	IGBT Gate
E1–E6	IGBT Gate return
C1–C6	Desat detect / collector sense
T11, T12	Phase 1 temperature sensor output
T21, T22	Phase 2 temperature sensor output
T31, T32	Phase 3 temperature sensor output

Creepage and Clearance Requirements

Care should be taken not to encroach on the creepage and clearance requirements of the module as specified in the product data sheet. Additional external components, like metal heatsinks, bus bars or fastening hardware can inadvertently reduce the creepage and clearance distances in the assembly. It is critical to check the assembly to ensure the minimum required creepage and clearance are met as shown in Figure 6.
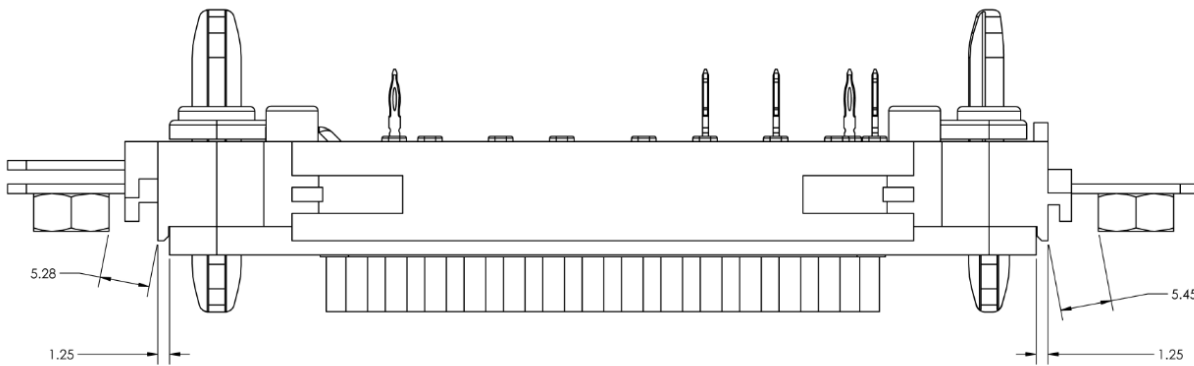

Figure 6. Creep and Clearance Distance for VE−Trac Direct Modules

THERMAL PERFORMANCE

Direct cooling offers a shorter path for heat to flow from the chip to the fluid. Since the module is direct cooled, there is no reason to use a thermal interface material. Below are thermal parameters of the IGBT and Diode from device junction to coolant fluid as shown in the data sheet below:

Table 2. BASIC THERMAL RESISTANCE AND IMPEDANCE CURVE IS PROVIDED FOR EACH MODULE TYPE IN THE DATA SHEET

Symbol	Parameter	Min.	Typ.	Max.	Unit
IGBT.$R_{th,J-F}$	Rth, Junction to Fluid, 10L/min, 65°C, 50/50 EGW		0.11	tbd	°C/W
Diode.$R_{th,J-F}$	Rth, Junction to Fluid, 10L/min, 65°C, 50/50 EGW		0.16	tbd	°C/W

The $R_{th,J-F}$ for the IGBT and Diode is measured using a reference cooling jacket and may vary slightly with different cooling jacket designs, flow rate, coolant temperature and coolant type. Please refer to the VE−Trac Direct assembly guide for more details on the reference cooling jacket and its sealing ring.

Thermal Measurements

The measurement of the thermal resistance is defined in the AQG324 standard. It uses the following equation to determine the steady state thermal resistance ($R_{th,j-f}$) for either the diode or the IGBT. The Tvj for the device is determined using the Vce or Vf method described in detail

in DIN EN60747−15. The test setup measures the inlet fluid temperature ($T_{f.in}$) and the outlet fluid temperature ($T_{f.out}$) to determine the average fluid temperature. This value is

then subtracted from the measured Tvj and divided by the power dissipated (P_d) in the device to determine the thermal resistance from junction to fluid.
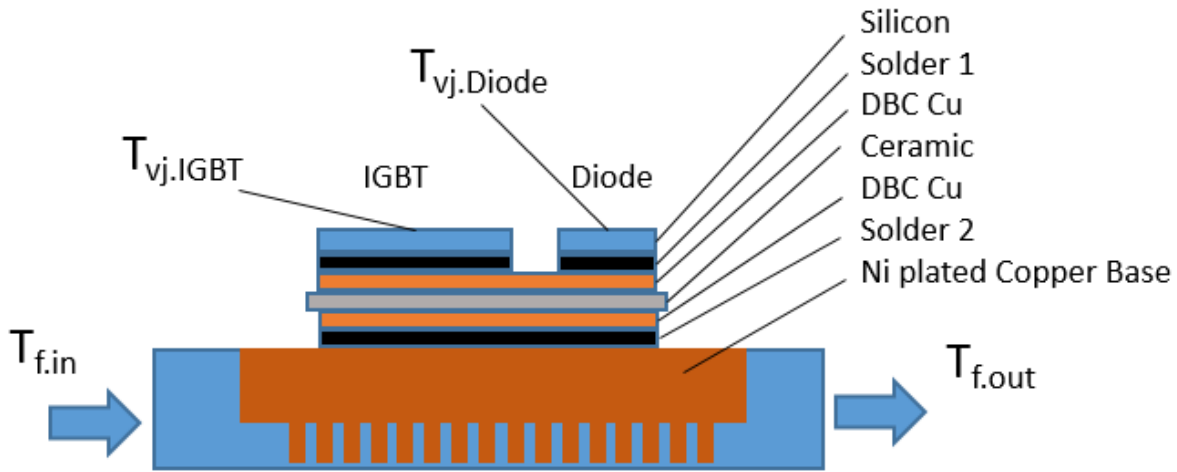

Figure 7. Thermal Stack up of a Typical VE−Trac Direct Module

$$R_{th,J-f} = \frac{T_{VJ} - \left(\frac{T_{f,in} + T_{f,out}}{2}\right)}{P_d} \quad \text{(eq. 1)}$$

Where:

Rth.j-f: Thermal resistance from device junction to fluid for IGBT or Diode

T_{vj}: Device junction temperature

$T_{f.in}$: Fluid inlet temperature

$T_{f.out}$: Fluid outlet temperature

P_d: Power dissipated in the device

Thermal Modeling

The information needed to develop circuit level or mathematical model for the power module is provided below. This includes the equivalent thermal impedance and thermal capacitance for a four node Foster thermal network for the electrical equivalent models and math expressions. It is important to note that the nodes are not related to material boundary or geometry of the physical thermal stack up as

shown in Figure 7. The information provided in the table below is also provided in the respective data sheet for the product. The table also includes the cross coupling thermal resistance between the IGBT and the free−wheeling diode (FWD) for the same side and also to the opposing side. It also shows the values between the high side IGBT and the low side IGBT devices. The strongest coupling to consider is between the IGBT and its FWD.

Table 3. FOUR NODE FOSTER MODEL EQUIVALENT RESISTANCE AND CAPACITANCE VALUES FOR THE 820 A, 750 V MODULE TYPE

Nodes	IGBT		Diode	
	Rth	**Cth**	**Rth**	**Cth**
Node 1	0.05071	1.64	0.0623	0.298
Node 2	0.00010	10503.8	0.0665	1.79
Node 3	0.01702	0.449	0.0104	0.12
Node 4	0.03958	17.75	0.0297	31.86
Total	0.107	–	0.169	–
x–coupling Rth IGBT <–> Diode IGBT <–> IGBT	0.036 (same side) n/a		0.008 (opposing side) 0.008 (opposing side)	

ELECTRICAL PERFORMANCE

This section explains the maximum, static and dynamic electrical parameters of the IGBT and Diode used inside the module. Each functional switch of the module consists of 3x IGBT and Diode chips connected in parallel. The parameters included in the data sheet refers to a functional switch and not a single chip. Maximum values of these parameters should not be exceeded, in normal operation to prevent damage to the semiconductor. In addition, please note that the temperature condition is 25°C, unless it is specified otherwise.

Maximum Ratings – IGBT

Operating Junction Temperature, T_{vj}

This is the junction temperature range where the device is guaranteed to operate without physical or electrical damage. Like similar automotive power modules the ratings, maximum Tvj includes a continuous rating and a short term higher rating. VE–Trac Direct specifies a continuous operational T_{vj} range –40°C to 175°C with no short duration rating.

Safe Operating Area of IGBT

The maximum allowed peak Collector to Emitter Voltage (V_{CES}) is specified at a junction temperature of 25°C. Please note this value has a positive temperature coefficient, meaning at lower temperatures the maximum allowed peak Collector to Emitter is also lower. There are two plots in the data sheet that should be checked to ensure safe operation of the module. The first plot is the Maximum V_{CE} rating over temperature as shown in Figure 8. This determines the absolute maximum allowed peak blocking voltage between the IGBT Collector–Emitter across the operating temperature range. Note that at –40°C the maximum V_{CE} rating is 715 V.

The second plot to consider is the Reverse Bias Safe Operating Area (RBSOA). This shows the peak V_{CE} allowed as a function of collector current at 150°C for the power module (see Figure 8). It shows the ideal SOA for the chip and also the module, which includes the module parasitic inductance. However, it's important to also consider all the parasitic inductance in the power loop (including DC filter capacitor) to determine the true SOA for the module in the end application.
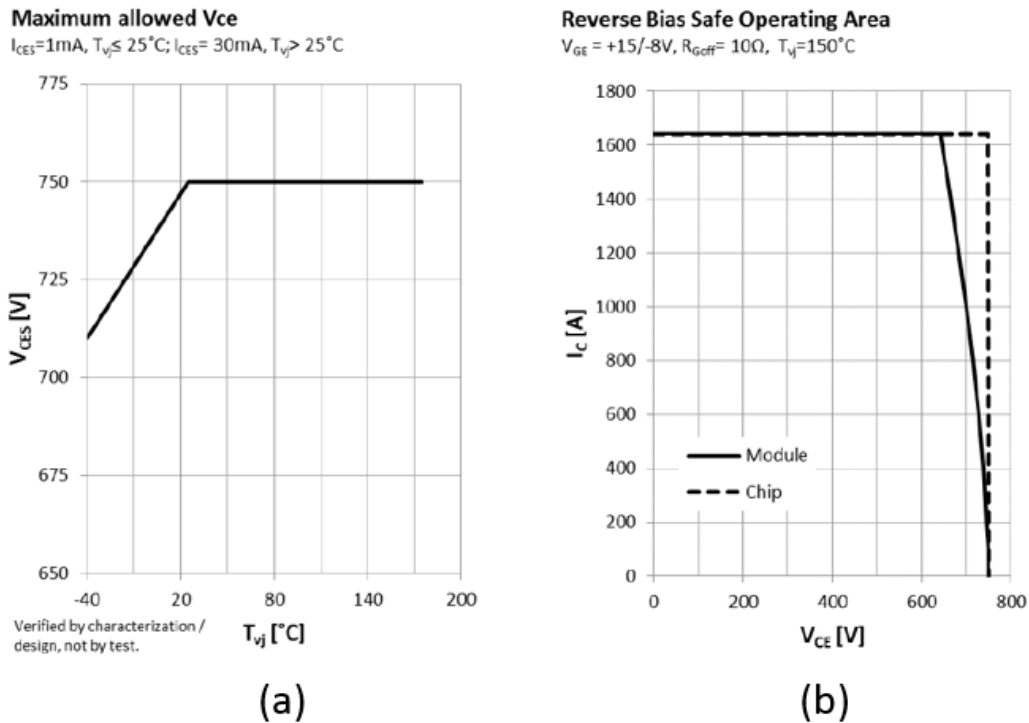
Maximum allowed Vce
I_{CES}=1mA, T_{vj}≤ 25°C; I_{CES}= 30mA, T_{vj}> 25°C

Verified by characterization /
design, not by test.

(a)

Reverse Bias Safe Operating Area
V_{GE} = +15/-8V, R_{Goff}= 10Ω, T_{vj}=150°C

— Module
--- Chip

(b)

Figure 8. (a) Vce versus Temperature (b) RBSOA for the 820 A, 750 V Module Type

Lastly, the SOA plot should be checked for pulsed conditions. The IGBT module must not be used in the linear mode. Figure 9 shows the IGBT current capability for single pulse events and for DC. This plot is not included in the data sheet. The DC rating in the plot is limited the continuous $T_{j.max}$ rating of 150°C, but the pulsed plot lines are limited by the $T_{j.max}$ value of 175°C.
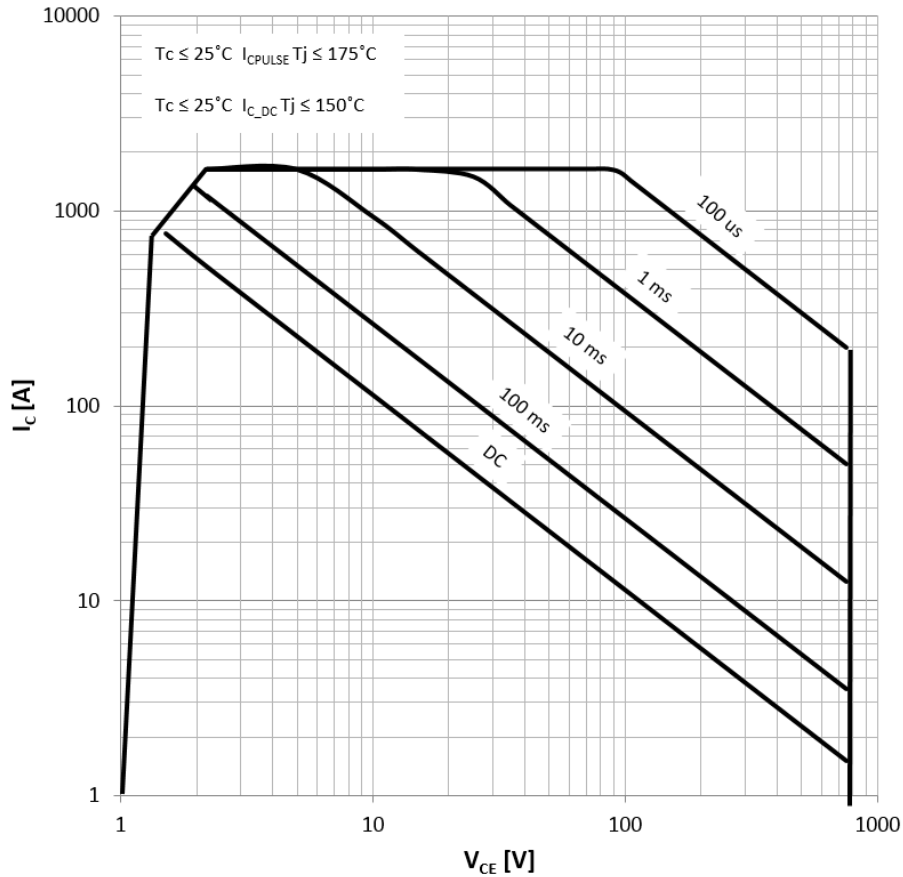
Figure 9. SOA for the 820 A, 750 V Module Type

Continuous DC Collector Current, Ic nom

Ic_nom is the continuous DC current allowed when using the reference heatsink which results in $R_{th,J-F}$ value specified in the data sheet. Ic nom is determined by three factors: Vcesat(as a function of T_{vj} and Ic), IGBT Junction to Fluid thermal resistance $R_{th,j-f}$ and Max Operating Junction temperature. A design margin is also applied to determine the final Ic nom value and it is verified by characterization testing where Tvj is determined according to IEC60747−15.

Maximum Pulsed Collector Current, ICRM

VE−Trac[TM] Direct modules specify ICRM as 2X of IGBT rating current at room temperature. When the fluid temperature is higher, pulse width should be determined by power dissipation and transient thermal impedance Zth to make sure Tvj is not exceeding 175°C.

Short Circuit Withstand Time, SCWT

SCWT of VE−Trac[TM] Direct modules is specified and verified according to AQG324 Type 1 short circuit (HSF: hard−switch−fault). The short circuit characteristics depend heavily on application specific parameters such as temperature, stray inductances/resistance and gate driver. During a short circuit event, the IGBT has to withstand high junction temperature due to high power dissipation and turns off safely. Below figure show short circuit test setup.
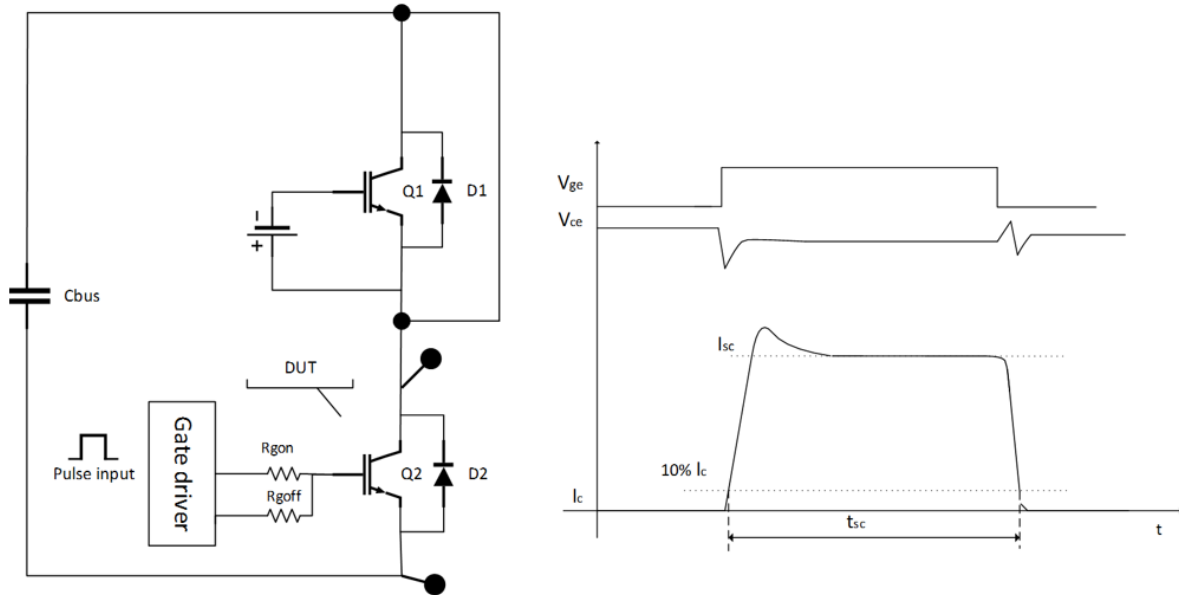
Figure 10. Short Circuit Measurement Circuit and SCWT Definition

Maximum Ratings – Diode

Repetitive Peak Voltage, VRRM

VRRM Voltage is maximum allowed reverse biased voltage for the diode. As IGBT and Diode are anti−parallel connected, diodes have to withstand the same voltage as the IGBT. The collector−Emitter voltage ratings in the data sheet will also apply for the anti−parallel diode.

Continuous Forward Current, I_F

Similar method of rating as the IGBT Ic nom. The continuous DC current rating for the diode is a little lower than the IGBT due to the higher $R_{th,J−F}$ value specified in the data sheet for the Diode. I_F value and it is verified by characterization testing where junction temperature is determined according to IEC60747−15.

Repetitive Peak Current, I_{FRM}

VE−Trac Direct modules specify I_{FRM} as 2X of I_{FN}. When the fluid temperature is higher, pulse width should be determined by power dissipation and transient thermal impedance Zth to make sure the Junction temperature is not exceeding 175°C

Surge Current Capability, I^2t value

Diode surge current is in the form of a half sine wave of 10ms or 8.3 ms (50 or 60 Hz), where its peak current is denoted as I_{surge}. The device is able to withstand this current without damage provided this does not occur too often in the diode service life. Instead of peak current, the datasheet specifies this characteristic in the form of I^2t value, given by:

$$\int_0^{tp} Idt = I_{surge}^2 * \frac{tp}{2} \qquad \text{(eq. 2)}$$

Where t_p is the pulse width.

Static Characteristics

IGBT Output characteristics, Vcesat

Vcesat is the voltage drop across collector to emitter for a specified gate voltage and temperature which is used to calculate IGBT's conduction losses and compare the losses between similar components. It is a temperature dependent parameter, as shown in Figure 11. Above the crossover, Vcesat exhibits positive temperature coefficient while below the crossover, it shows negative temperature coefficient. Positive temperature coefficient is beneficial in a way that it helps achieve better current sharing for paralleling operation.
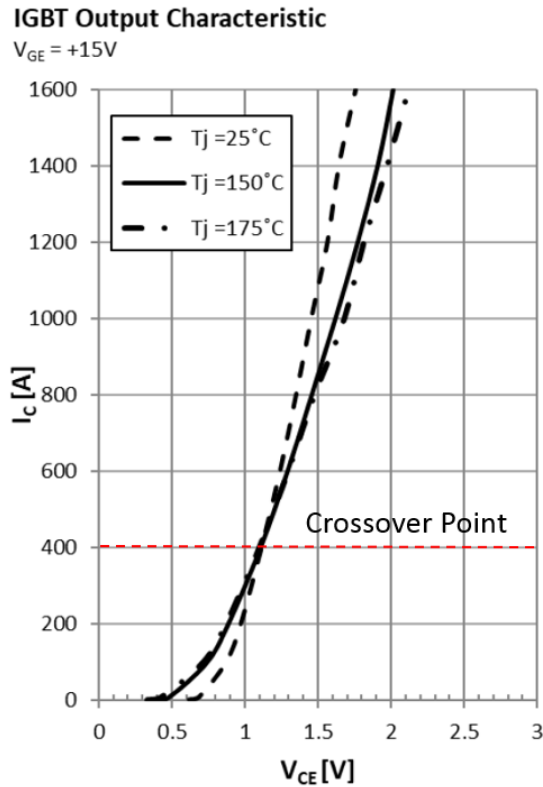
IGBT Output Characteristic
$V_{GE} = +15V$

Figure 11. Typical IGBT Output Characteristic Curve Showing the Crossover from NTC to PTC

Collector to Emitter Leakage Current, I$_{CES}$

I$_{CES}$ is the leakage current from collector to emitter when IGBT is turned off. It is highly related to the IGBT chip size and features a positive temperature coefficient−−− I$_{CES}$ increases when temperature is increasing.

Gate to Emitter leakage current, I$_{GES}$

The absolute maximum value of gate to emitter leakage current is typically specified at a gate voltage of 20V while collector and emitter are grounded. Typically only the maximum value is specified in the data sheet and is in the order of a few hundred Nano amperes. The exact value is defined the respective product data sheet.

Threshold Voltage, V$_{th}$

V$_{th}$ indicates at what Vge voltage level the IGBT starts to conduct. It is tested by shorting Gate and Collector and applying a specified current source (e.g 5 mA) to collector.

Diode Forward Voltage, V$_F$

Diode forward voltage is measured when IGBT is in off−state. A forcing current is applied to the power pins of the module and the V$_F$ is measured through sensing pins. This helps eliminate the voltage drop effect along the current path (e.g wire, terminals) except the diode itself. Datasheet provides V$_F$ in a table with specified condition and curves at different temperatures and current.

Dynamic Characteristics

Parasitic Capacitances, Cies Coes Cres

As inherent parts of an IGBT device, several parasitic capacitances play a role in the device's dynamic characteristics including: input capacitance Cies, output capacitance Coes and reverse transfer capacitance Cres.
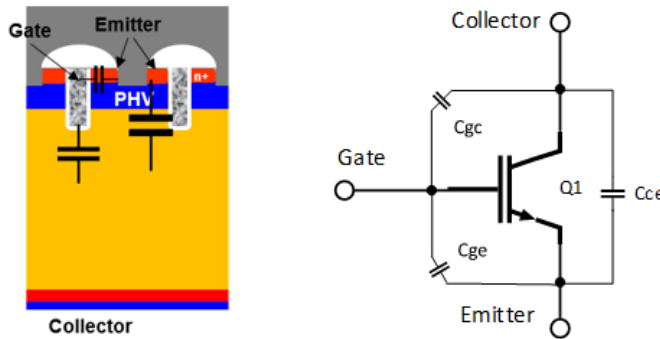
Figure 12. Parasitic capacitance in an IGBT.

Input Capacitance, Cies=Cge+Cgc

Input capacitance is formed by parallel combination of gate−to−emitter and gate−to−collector. The gate−to−emitter consists mainly of the metal−oxide−semiconductor capacitance and is generally constant. However gate−to−collector capacitance is voltage VCE dependent.

Output Capacitance, Coes=Cce+Cgc

Output capacitance is formed by parallel combination of collect−to−emitter and gate−to−collector, both of which are voltage dependent and varies with different collector−to−emitter voltages.

Reverse Transfer Capacitance, Cres=Cgc

Made up of gate−to−collector capacitance, reverse transfer capacitance plays an essential role in gate driving of

the IGBT, as it provides negative feedback from collector to gate and is responsible for the gate voltage plateau. Specifically, during IGBT turning on, the fast falling of collector−to−emitter voltage forms a considerable current from collector to gate through Cres which counteracts the rising of the gate voltage. Similarly, during IGBT turning off, the fast rising of collector−to−emitter voltage draws current from gate through Cres which counteracts the falling the gate voltage. Coes and Cres tend to decrease when V_{CE} voltage is increasing while Cies is mostly stable across different V_{CE} voltages. Figure 13 shows a typical Capacitance vs V_{CE} Curve for a 750 V VE−Trac Direct IGBT.
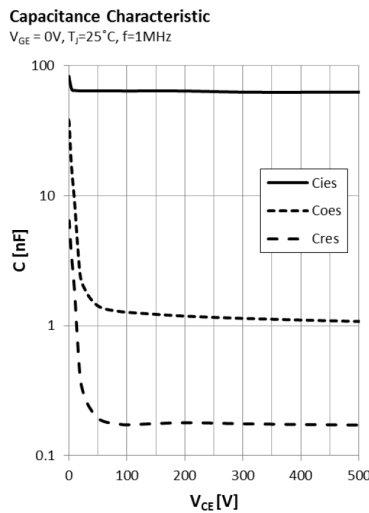

Figure 13. Typical Parasitic Capacitance Curves versus Vce

Press−fit pin Inductance

The inductance of the press−fit connection is calculated with a modeling tool that considers the geometry and material properties of the module. $L_{P.GE}$ represents the inductance of the gate press−fit pin, DBC tracks, wire bonds

and the gate return press−fit pin. In typical gate driver applications, one should also consider the PCB track inductance to get the complete gate−emitter loop inductance.
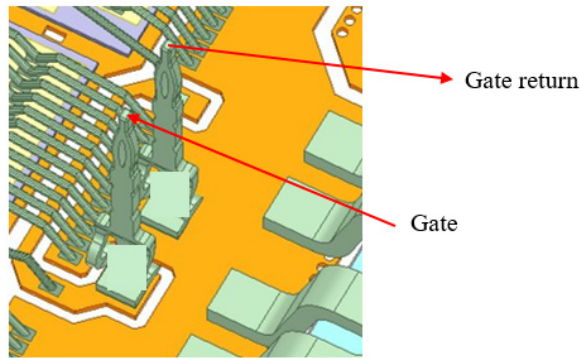
Figure 14. Press−fit Gate Loop

Table 4. PRESS−FIT GATE−EMITTER LOOP INDUCTANCE CALCULATED USING FEM TOOL

SWITCH POSITION	$L_{P.GE}$(nH)@1mHZ	$L_{P.GE}$(nH)@10 mHz
UPPER SWITCH	12.5	11.8
LOWER SWITCH	8.5	8.0

Gate Charge, Q_G

Though input capacitance is useful, gate charge provides a more convenient way in determining the average driving power for the IGBT. Specifically, the driving power is determined by following equation:

$$P_{gd} = f_s * Q_G * \left(V_{ge(on)} - V_{ge(off)} \right) \qquad \text{(eq. 3)}$$

Where f_s is switching frequency, $V_{ge(on)}$, $V_{ge(off)}$ are on−state gate−to−emitter voltage and off−state gate−to−emitter voltage respectively.

Besides a Q_G value at a certain V_{ge} condition, the datasheet also provides a Q_G curve where different Q_G vs V_{ge} information can be found. Refer to below figure for a typical Q_G curve. See section on gate drive to see how Q_G is used to determine gate driver requirements.
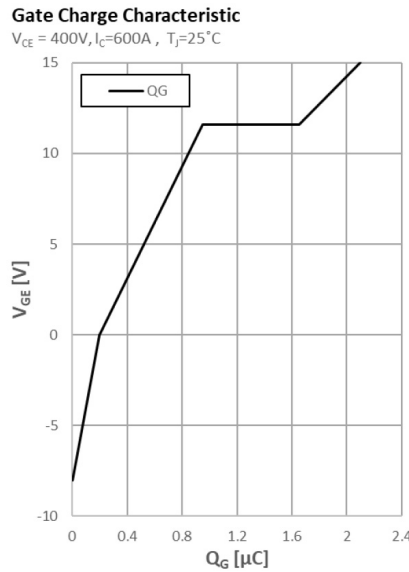
Figure 15. Example Gate Charge Characteristic of the 820 A, 750 V Module Type in Data Sheet

IGBT Switching Characteristics

IGBT switching characteristics are one of the major focuses in improving IGBT performance as switching losses constitute substantial part of overall losses. The circuit diagram used in characterizing IGBT switching behavior is shown in Figure 16.

IGBT Switching Characteristics are given in two types: one type is measured in time dimension −−− delay time and rise/fall time, this information is useful in determining an appropriate dead time between turn−on and turn−off of high and low side IGBTs in a half bridge configuration. Another type is measured in losses −−− turning on/off losses at room

and high temperatures under a given condition, such as Bus voltage, Gate resistance and Gate voltages etc. This information is useful in estimating switching losses in real application and compare performances of devices from different suppliers.
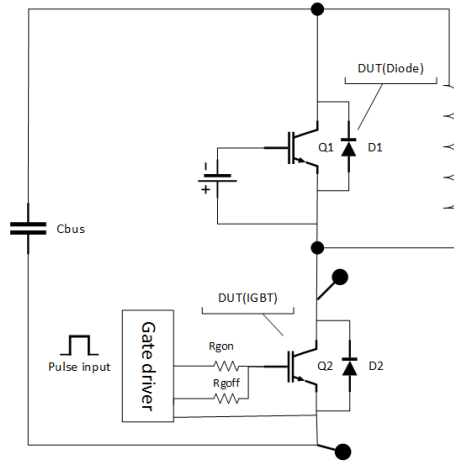

Figure 16. Double Pulse Test Set−up for Dynamic Measurements

The definitions for IGBT switching characteristics are explained as below:

a. Turn on delay time, $T_{d.on}$
Time interval from the moment when gate−emitter voltage reaches to 10% of rated value to the moment when collector current reaches 10% of its nominal value.

b. Turn off delay time, $T_{d.off}$
Time interval from the moment when gate−emitter voltage drops to 90% of rated value to the moment when collector current drops to 90% of its nominal value.

c. Rise time, T_r
Time it takes for collector current to rise from 10% to 90% of its nominal value.

d. Fall time, T_f
Time it takes for collector current to fall from 90% to 10% of its nominal value.

e. Turn−on switching losses E_{on},
Turn−on switching losses are integral of power−−Collect−to Emitter voltage multiplying Collector current −−−− over the time interval starting when the collector current reaches 10% of its final value and ending when collector−emitter voltage drops to 2% of IGBT's off−state value, illustrated as below equation:

$$E_{on} = \int_{t1}^{t2} V_{CE} * I_C * dt \qquad \text{(eq. 4)}$$

f. Turn−off losses, E_{off}
Turn−off switching losses are integral of power−−Collect−to Emitter voltage multiplying Collector current −−−− over the time interval starting when collector−emitter voltage reaches 10% of its final value and ending when collector current drops to 2% of IGBT's on−state value, illustrated as below equation:

$$E_{off} = \int_{t3}^{t4} V_{CE} * I_C * dt \qquad \text{(eq. 5)}$$

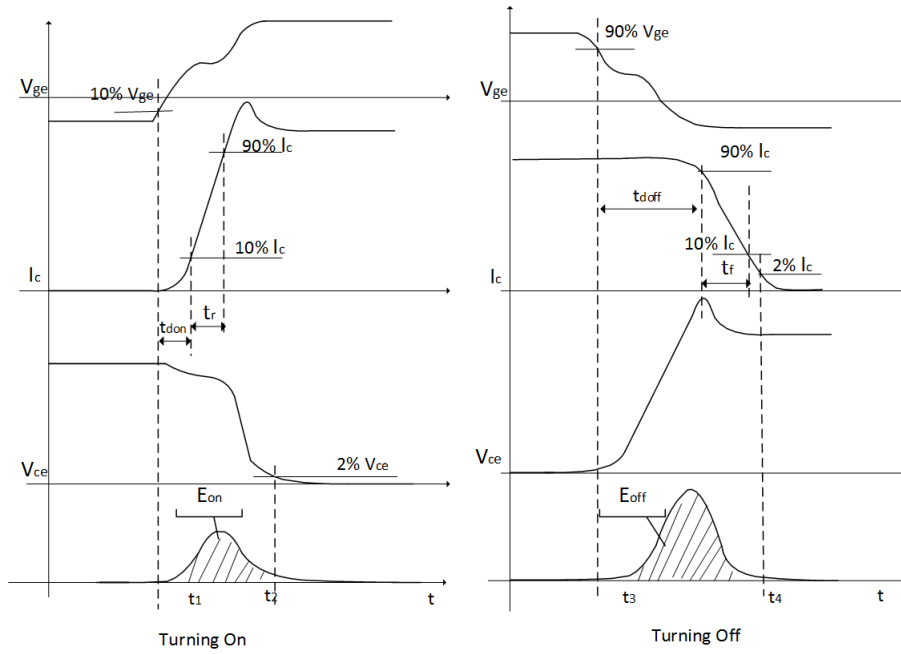In Figure 17 the definitions of the terms with respect to the waveforms are illustrated:

Figure 17. Switching Parameter Definitions for the IGBT

Diode Switching Characteristics

When the diode is switched from forward current carrying to reverse voltage blocking by turning−on of the opposite side IGBT, it enters the Reverse Recovery State. Refer to Figure 18 for double pulse testing configuration and definition of diode reverse recovery parameters.
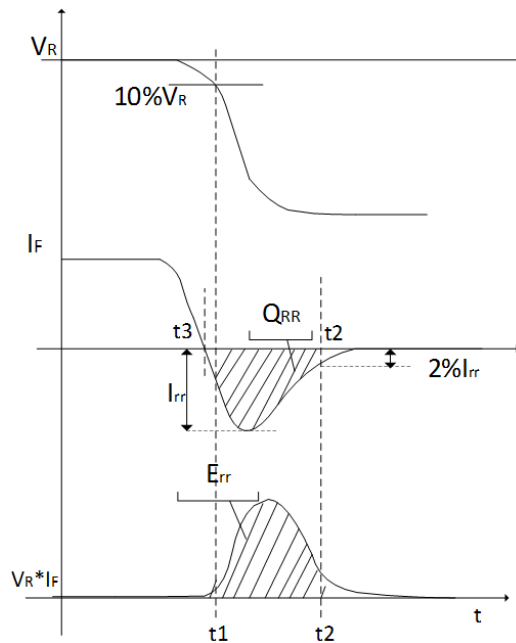

Figure 18. Switching Parameter Definitions for the Diode

a. Reverse Recovery Current, I_{rr}

Reverse recovery current is the peak current when the diode current is commutated from forward conducting to reverse bias. It depends on the initial forward diode current and current slope rate — di/dt.

b. Reverse Recovery Charge, Q_{rr}

Reverse recovery charge is the amount of charge that is recovered from the diode during turning off. It is calculated by integrating the reverse recovery current over the time period starting when diode current crosses zero and ending when diode

reverse current return to 2% of its peak reverse current(I_{rr}). Shown as below equation:

$$Q_{rr} = \int_{t3}^{t2} I_F dt \qquad \text{(eq. 6)}$$

c. Reverse Recovery Energy, E_{rr}

Diode reverse recovery energy are integral of power—Diode reverse voltage multiplying diode reverse current ———— over the time interval starting when reverse voltage reaches 10% of its final value and ending when reverse current returns to 2% of its reverse recovery peak current, illustrated as below equation:

$$E_{rr} = \int_{t3}^{t2} V_R * I_F dt \qquad \text{(eq. 7)}$$

INTEGRATED THERMISTORS

Each VE–Trac Direct power module includes an NTC thermistor mounted on each phase of the 6–pak module. The thermistor is located on top of the DBC substrate close to the chips of the upper switch as shown in Figure 19. The thermistor response can be used to implement over temperature protection or other fault indications like loss of coolant flow. However, it be noted that the response time of the thermistor is in the order of ~300 ms and thus will not detect fast chip temperature variations.
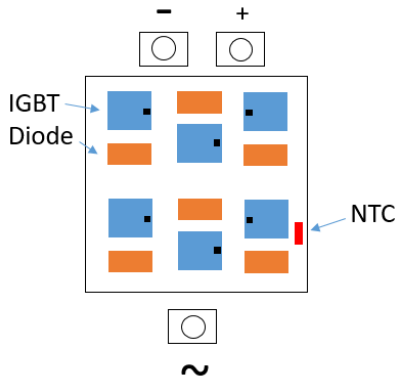
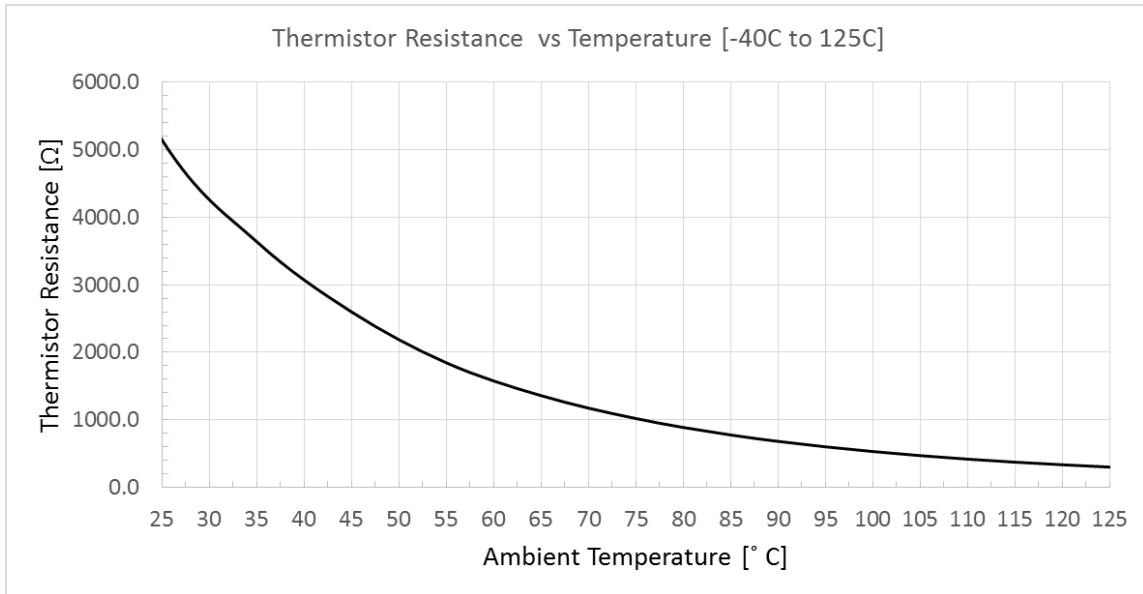**Figure 19. Approximate Location of the NTC Thermistor on Each Phase Leg**

Figure 20. NTC Thermistor Resistance versus Temperature

Table 5. TOLERANCE OF THE NTC THERMISTOR AT VARIOUS TEMPERATURES

Ambient Temperature [°C]	Typ Resistance[kΩ]	Tolerance [±%]
−40	99.090	17%
−35	75.170	16%
−30	57.540	16%
−25	44.440	15%
−20	34.600	14%
−15	27.260	13%
−10	21.480	13%
−5	17.110	13%
0	13.720	12%
5	11.080	12%
10	9.000	11%
15	7.357	11%
20	6.048	10%
25	5.000	10%
30	4.156	9%
35	3.471	9%
40	2.914	9%
45	2.458	8%
50	2.083	8%
55	1.772	8%
60	1.515	7%
65	1.300	7%

Table 5. TOLERANCE OF THE NTC THERMISTOR AT VARIOUS TEMPERATURES (continued)

Ambient Temperature [°C]	Typ Resistance[kΩ]	Tolerance [±%]
70	1.120	7%
75	0.968	6%
80	0.840	6%
85	0.732	6%
90	0.640	6%
95	0.561	5%
100	0.493	5%
105	0.435	5%
110	0.385	6%
115	0.342	6%
120	0.304	6%
125	0.271	6%
130	0.243	6%
135	0.218	7%
140	0.196	7%
145	0.177	7%
150	0.160	7%
155	0.144	7%
160	0.131	8%
165	0.119	8%
170	0.109	8%
175	0.099	8%

$$T.NTC[°C] = \frac{1}{\left(\ln\left(\frac{R.NTC}{R25}\right)\right) + \left(\frac{1}{298.15k}\right)} - 237.15k \qquad (eq.\ 8)$$

$$R.NTC[\Omega]R25 * \exp\left(B * \left(\frac{1}{273.15k + T.NTC} - \frac{1}{298.15k}\right)\right) \qquad (eq.\ 9)$$

Where:

T.NTC: The thermistor resistance converted to temperature of thermistor

R.NTC: The thermistor resistance in ohms

B: The beta value from data sheet

R25 or R_{25}: Thermistor resistance at 25°C from data sheet

The relationship between the Thermistor resistance and the Tvj of the IGBT and Diode are described in Table 6 for a specific operating condition for the 750 V, 820 A module. Users will need to make similar measurements to develop the relationship or equation for their specific operating condition. This is necessary to have a robust over temperature protection scheme. It should be noted that for the data shown in Table 6 the devices are heated separately i.e. when the IGBTs are conducting the diodes are not conducting and vice−versa.

Table 6. EXAMPLE RELATION BETWEEN NTC THERMISTOR TEMPERATURES TO DEVICE JUNCTION TEMPERATURE FOR A SPECIFIC OPERATING CONDITION FOR THE 820 A, 750 A MODULE

Coolant@65C, 10L/min, Ref. Cooler. DC current only in IGBT			Coolant@65C, 10L/min, Ref. Cooler. DC current only in FWD		
Tvj.IGBT [C]	Thermistor.Resistance [KOhms]	Thermistor.Temperature [C]	Tvj.Diode [C]	Thermistor.Resistance [KOhms]	Thermistor.Temperature [C]
65	1.36	65	65	1.36	65
76.8	1.215	68.75	84	1.224	68.49
89.3	1.122	71.54	106.9	1.146	70.79
104.3	1.017	75.04	133.5	1.066	73.35
121.9	0.912	79.01	150	1.019	74.97
142.1	0.81	83.44	175	0.96	77.13
150	0.775	85.12			
175	0.678	90.29			

DESIGN CONSIDERATIONS

Gate Driver

The gate driver turns on and off the IGBT to a defined VGE_ON and VGE_OFF voltage levels. The transition between the two gate voltage levels needs a power to be dissipated in the gate driver. The gate driver power rating should be selected according to driver power required for an IGBT module.

The gate driver power required depends on QG – total gate charge of an IGBT module, switching frequency Fsw and the gate driver output voltage swing ΔVGE (VGE_ON – VGE_OFF).

$$P_{gd} = Q_G * F_{SW} * \Delta VGE \qquad \text{(eq. 10)}$$

If an external CGE is connected then the Power required for charging and discharging the external CGE should also to be considered.

$$\text{(eq. 11)}$$
$$P_{gd} = Q_G * F_{SW} * \Delta VGE + CGE * F_{SW} * \Delta VGE2$$

The switching speeds of an IGBT are controlled by charging and discharging rate of the gate capacitances, Higher the peak current, lower are the losses. Other switching factors like overvoltage stress and peak reverse recovery current of freewheeling diode has a direct impact on this. The turn−on and turn−off peak gate currents are controlled by resistors RG,ON and RG,OFF respectively (see Figure 21).
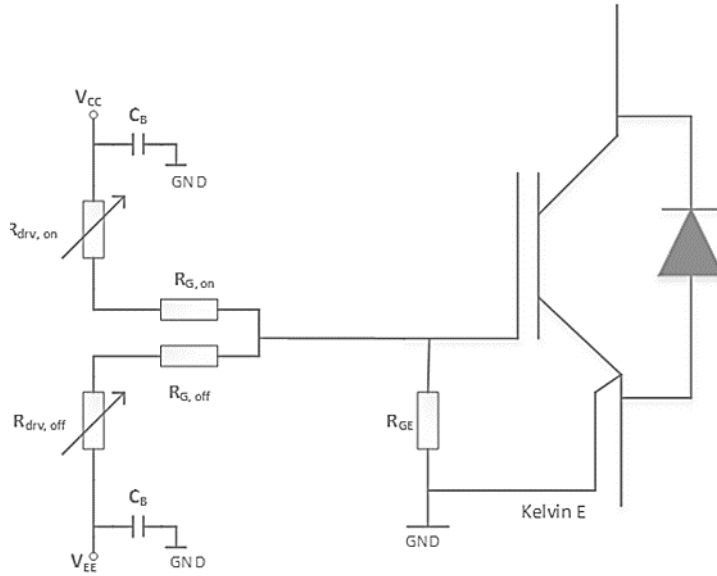
Figure 21. Basic Gate Drive Circuit

$$I_{GPEAK-ON} = (V_{CC} - V_{EE})/(R_{G,ON} + R_{G,INT} + R_{drv,on})$$ (eq. 12)

$$I_{GPEAK-OFF} = (V_{CC} - V_{EE})/(R_{G,OFF} + R_{G,INT} + R_{drv,off})$$ (eq. 13)

The average current needed for switching an IGBT at switching frequency of Fsw and total gate charge Q_G can be calculated as follows:

$$I_{G(AVG)} = Q_G * F_{SW}$$ (eq. 14)

The gate driver continuous current rating should be > $I_{G(AVG)}$ calculated.

The peak charging and discharging rate of gate currents to the input capacitance of an IGBT module results in power dissipation in the gate resistors. The gate resistor must be sized to handle this power dissipation. The peak charging or discharging current can be approximated as a discontinuous triangular wave.

$$P_{RG} = (2/3) * I_{GPEAK}{}^2 * T_P * F_{SW} * R_G$$ (eq. 15)

Where:

I_{GPEAK} :IGBT Gate drive peak current

T_p: Duration of the pulse usually between 500 ns to 1 μs

Fsw:IGBT switching Frequency

R_G: Gate resistance

Sometimes there is significant ringing on the gate drive loop. The gate driver equivalent circuit with parasitic is as shown below.
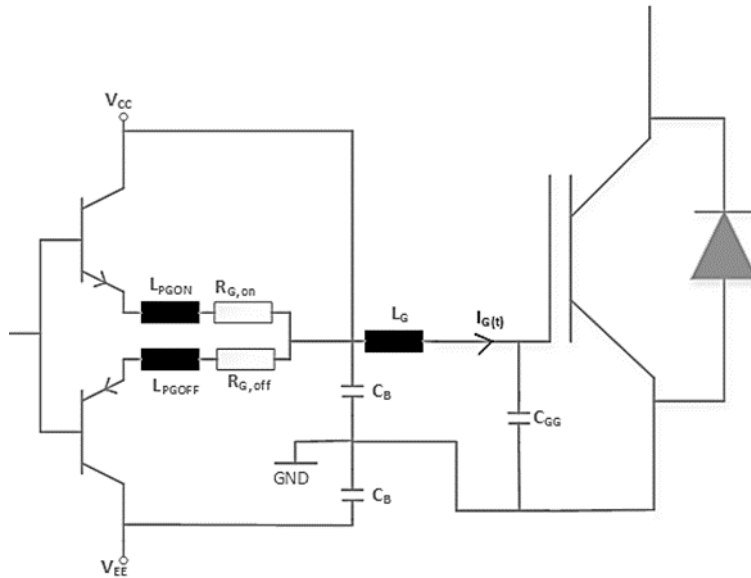
Figure 22. Gate Drive Circuit Shown with Parasitic.

The gate current is $I_G(t)$ is related to known second order differential equation for RLC circuits. During turn –on L_T and R_T represent total inductance and resistance in the turn−on path

$$L_T = L_{PGON} + L_G \qquad \text{(eq. 16)}$$

$$R_T = R_{G,ON} + R_{GINT} \qquad \text{(eq. 17)}$$

The minimum value of R_T required for non−oscillation or for over damped condition is $R_T = R_{G,ON} + R_{GINT} > 2 *$ $S_{QRT}(L_T/C_{GG})$

During turn−off L_{TF} and R_{TF} represent total inductance and resistance in the turn off path of the gate loop.

$$L_{TF} = L_{PGOFF} + L_G \qquad \text{(eq. 18)}$$

$$R_{TF} = R_{PG,OFF} + R_{GINT} \qquad \text{(eq. 19)}$$

The minimum value of R_{TF} required to prevent oscillation or for over damped condition is $R_{TF} = R_{G,OFF} + R_{GINT} > 2 * S_{QRT}(L_{TF}/C_{GG})$

Uni−Polar versus Bi−Polar Drive

The unipolar gate drive switches on the IGBT with voltage VGE_ON (typically +15V) and turns off the IGBT

voltage with 0V. This arrangement is not recommended for EV traction drive applications, since it tends to increase switching losses and increase EMC susceptibility. However, if a uni−polar drive is desired, the following precautions should be considered:

1. Parasitic Turn on due to miller capacitor and high dv/dt
2. Parasitic turn on via stray inductances

Parasitic turn−on via stray inductance can be common when there is no kelvin emitter sense, in which case the gate driver reference shares the same reference as the power emitter.

In the Inverter half bridge application when the low side IGBT turns−on, a high side IGBT experiences a voltage rise dvce/dt. This causes a displacement current ICGC = CGC*dvce/dt to flow through the miller capacitor and RG,off of the upper IGBT and back into the driver as shown in Figure 23. As a result VGE rises when it exceeds the VGE(th) parasitic turn−on of the high side IGBT. This can result in a shoot−through event i.e short across the DC link.
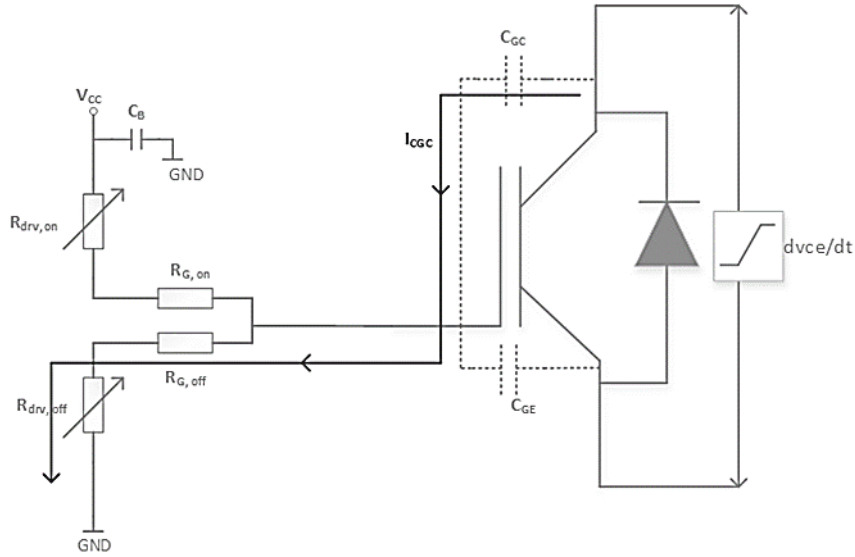
Figure 23. Parasitic Turn–On Due to Miller Capacitor and High dv/dt

$$V_{GE} = I_{CGC} * \left(R_{G,off} + R_{drv,off} + R_{GINT}\right) \quad \text{(eq. 20)}$$

A shoot event through can destroy the module. Thus when designing a gate driver circuit, maximum allowed dv/dt has to be considered. The maximum allowed dv/dt can be calculated as follows:

$$\frac{d_{VCE,max}}{dt} > \frac{V_{th}}{C_{GC} * R_{G,tot}} \quad \text{(eq. 21)}$$

Where Vth is the threshold voltage of IGBT for VE–Trac Direct. Vth is equal to 5.5 V and CGC is the Miller capacitance of the IGBT and is equal to 1.3nF (for example). Thus from above equation the maximum allowed dv/dt for VE–TracTM Direct will be:

$$\frac{d_{VCE,max}}{dt} \leq \frac{4.2}{R_{G,tot}} \; (V/ns) \quad \text{(eq. 22)}$$

Where RG, tot is the total gate resistance during turn off event.

In order to increase the robustness of unipolar gate drive against the parasitic miller capacitor turn–on, consider using an Active Miller Clamp circuit where during turn–off the VGE voltage is monitored internally within the gate driver. When the voltage VGE falls below 2 V relative to the emitter reference, the clamp circuit is activated. This clamp switch (see Figure 24) shorts the Gate Emitter terminals of an IGBT and shunts all the miller displacement current into it, thereby reducing the VGE below the threshold voltage VGETH.
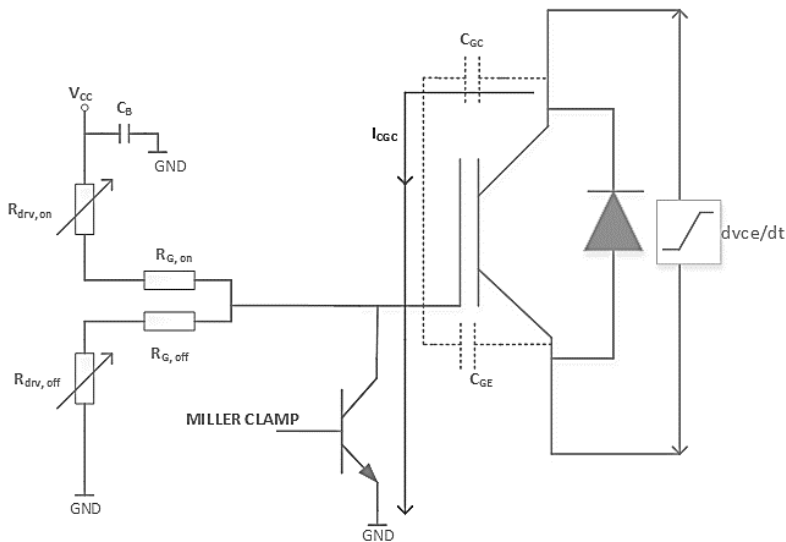
Figure 24. Example use of miller clamp to prevent unintended Turn–On.

Parallel Operation

The VE−Trac Direct family of modules are in 6−pak configuration and is designed to be used as standalone modules in 3−phase inverter applications. Although, they can be paralleled for higher power applications, the VE−Trac Dual family of half−bridge modules represent a more cost effective option for paralleling.

RELIABILITY

Module Life Estimation

Power module lifetime can be determined from power cycle capability curves. However, since the power module has currently not completed qualification, this data is not available yet. The lifetime reference curves will be added when the product is fully qualified. The VE−Trac Direct modules are expected to be at par or better than similar modules in the market today.

Qualification Tests

The objective of the qualification tests are to ensure general product quality and reliability. The product use the requirements set in the AQG324 document as its minimum requirements and in some cases will exceed these requirements.

Table 7. SUMMARY OF QUALIFICATION TESTS

Test	Standard	Test Conditions
High Temp Reverser Bias	AQG324	T_J = 175°C, Bias = 80% VCE
High Temp Gate Bias	AQG324	T_J = 175°C, Bias = 20 V for +, V_{CE}=0, V_{GE} = negative mean for gate
High Temp / Low Temp Storage Life	JESD22−A101	Per JESD standards
Temperature Humidity Unbiased	JESD22−A101	Per JESD standards
High Humidity High Temperature Reverse Bias	JESD22−A101	Per JESD standards
Temperature Cycling & Vibration & Shock	AQG324, LV124, JESD22−A104	−40 to +125°C
Power Cycling Test	AQG324	Multiple PCmin & PCsec conditions defined to meet the requirements in the standard.
Vibration Variable Frequency	JESD22−B103	25−500 Hz/15 min, 10G, 2hrs, XYZ
Package drop	EIAJ−ED−4701 A124	75 cm onto 3 cm maple board 3x
Solderability	JESD22−B102	T_A = 254°C 20 sec dwell
Customer Destructive Physical Analysis	AEC Q101	Per 100TC, 100TS, 20k PCT
ESD Characterization	AEC Q101−001 and −005	HBM, CDM
Die Shear & Wire Bond Pull & Wire Bond Shear	MIL−STD883 Method 2019/2011 & AEC−Q101−003	Per Assembly Spec

VISUAL MARKINGS

Traceability and Identification

For automotive applications, proper identification of materials and traceability is an important aspect of quality.

Standard markings for the power module is shown below in Figure 25 and explained in Table 7.
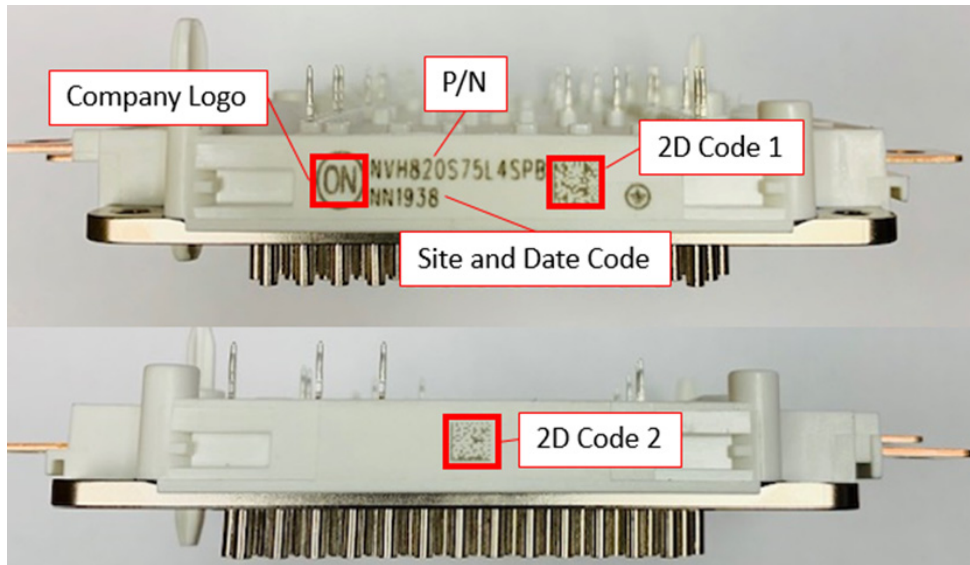
Figure 25. Module Identification Labels and Markings

The 2D Code is readable with most 2D scanners compatible with the IEC 24720 and IEC 16022 standard.

Certain apps for reading QR codes on android smart phones can also read the 2D codes on the module.

Table 8. EXPLANATION OF VISUAL MARKINGS ON THE MODULE

Marker	Description
COMPANY LOGO	**onsemi** Logo
2D CODE 1	Date Code (YYWW) + Assembly Location (XX) + Assembly Lot Number + S/N
2D CODE 2	Assy. Lot Number + S/N
SITE AND DATE CODE	Assembly location (XX) and date code (YYWW)
P/N NUMBER	14 Character Product part number

Storage and Shipping

Transporting and storing the modules requires care to avoid extreme shock, vibration and environments. The recommended storage conditions for the module according to IEC 60721−3−1, class 1K2 should be followed and storage time should not exceed 2 years. Below is a summary of the recommended storage parameters:

Table 9. STORAGE AND SHIPPING CONDITIONS

Maximum air temperature	40	°C
Minimum air temperature	+5	°C
Maximum relative humidity	85	%
Minimum relative humidity	5	%
Condensation	Not Allowed	
Precipitation	Not Allowed	
Icing	Not Allowed	

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PUBLICATION ORDERING INFORMATION

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