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AND9800/D

Automotive Smart Power Module, 650 V ASPM27 Series

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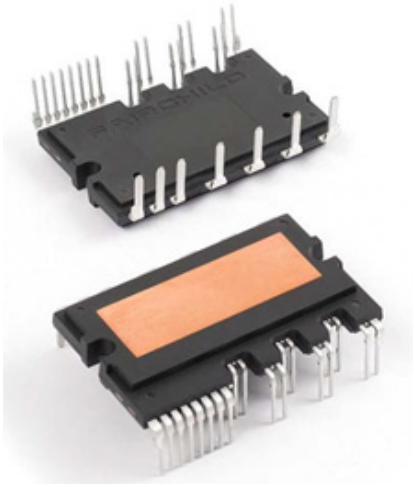
APPLICATION NOTE



SPMCA−027 / PDD STD, SPM27−CA, DBC TYPE CASE MODFJ

INTRODUCTION

The 650 V ASPM27 series extends the existing Intelligent Power Module product portfolio, qualifying them to meet the performance and reliability requirements of automotive auxiliary motor drives in Hybrid and Electric Vehicle application. This application note supports the 650 V ASPM27 series. It should be used in conjunction with the 650 V ASPM27 datasheets and application note AN−9086 (Mounting Guidance).

Design Concept

The 650 V ASPM27 design objective is to provide a minimized package and a low power consumption module with improved reliability. This is achieved by applying new gate−driving High−Voltage Integrated Circuit (HVIC), a new Insulated−Gate Bipolar Transistor (IGBT) of advanced silicon technology, and improved Direct Bonded Copper (DBC) substrate base transfer mold package. The 650 V ASPM27 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for Automotive use, such as E−compressor, Oil pump, Fuel pump, Water pump, cooling fans and other auxiliary motors in Hybrid and Electric Vehicles.

The temperature sensing function of the 650 V ASPM27 products is implemented in the LVIC to enhance the system reliability. An analog voltage proportional to the temperature of the LVIC is provided for monitoring the module temperature and necessary protections against over−temperature situations. The right figure shows the package outline structure.

Features

- Automotive Qualified (AEC−Q100, Q101 and AQG324)
- 650 V ASPM27, 3−Phase IGBT inverter with Integral gate drivers and protection
- Very Low Thermal Resistance by Adopting DBC Substrate
- Separate Open−Emitter pins from Low−Side IGBTs for Three−Phase current sensing
- Built−in Temperature Sensing Unit of IC
- Isolation Rating of 2500 V_{RMS}/1 min
- Pb−Free and RoHS compliant

PRODUCT DESCRIPTION

Ordering Information

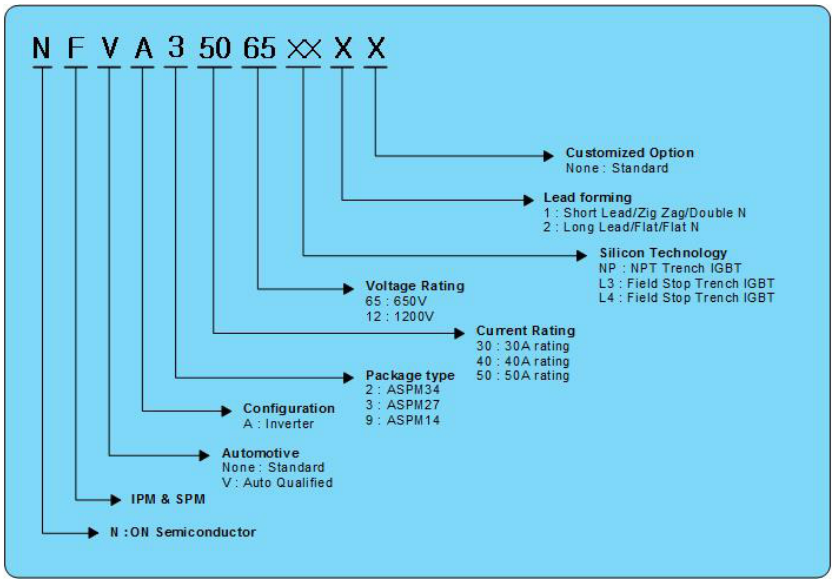


Figure 1. Ordering Information

Product Line−Up

Table 1 shows the basic line up without package variations. Online loss and temperature simulation tool, Motion Control Design Tool is recommended to find out the right the 650 V ASPM27 product for the desired application.

Table 1. PRODUCT LINE−UP

Target Application	Device	IGBT Rating	Motor Rating (Note 1)	Isolation Voltage	Remark
E−compressor, Oil pump, Fuel pump, Water pump, Cooling Fans	FAM65V05DF1	50 A/650 V	7 kW	V_{ISO} = 2500 V_{RMS} (Sine 60 Hz, 1−min All Shorted Pins Heat Sink)	Version 1.0
	NFVA33065L32	30 A/650 V	4.2 kW		Version 2.0
	NFVA34065L32	40 A/650 V	5.5 kW		
	NFVA35065L32	50 A/650 V	7 kW		

1. These motor ratings are general ratings, so may be changed by the operation conditions.

ASPM27 Version Comparison

As it can be seen from Table 2, the 650 V ASPM27 have two kinds of version. Old version (version 1.0) products have only one product. This ASPM27 version 2 is the first version in which all the line−up was released at the same with consistent features.

Table 2. ASPM27 VERSION COMPARISON

Version		Version 1	Version 2
IGBT Silicon Tech		Trench Field Stop IGBT	Trench Field Stop IGBT
Substrate		DBC (ALN)	DBC (Al2O3/ALN)
Current Rating / V_{CESAT}	30 [A]	−	NFVA33065L32 / 1.60 [V]
	40 [A]	−	NFVA34065L32 / 1.50 [V]
	50 [A]	FAM65V05DF1	NFVA35065L32 / 1.65 [V]
V_S−Output		Inner Bonding	Inner Bonding
OC/UV Protection		Yes	Yes
Thermal Sensing		Yes	Yes

PACKAGE

Internal Circuit Diagram

There is the internal circuit diagram of the 650 V ASPM27 as shown in Figure 2.

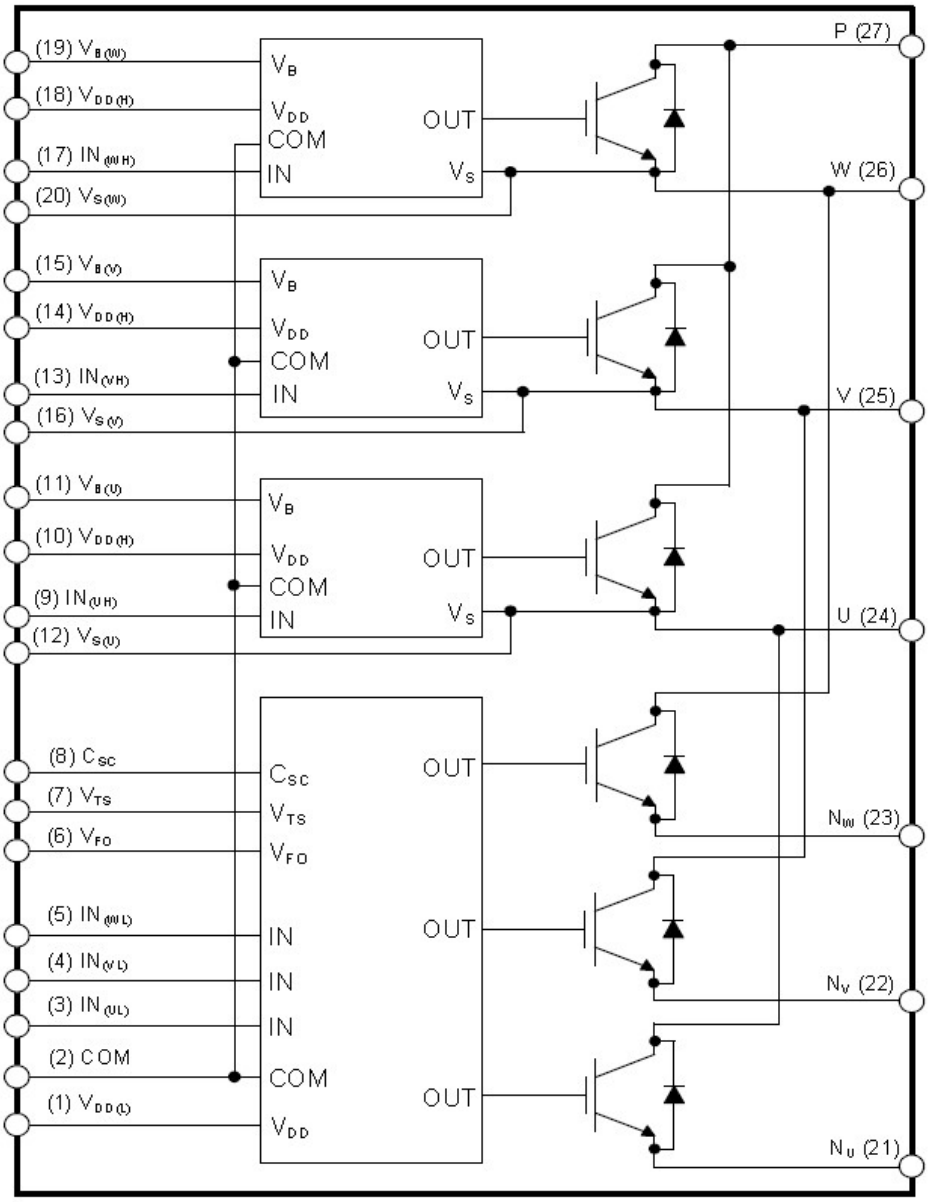


Figure 2. The 650 V ASPM27 Version Internal Circuit

Pin Description

Figure 3 shows the location of pins, the names and dummy pins of the 650 V ASPM27 series.

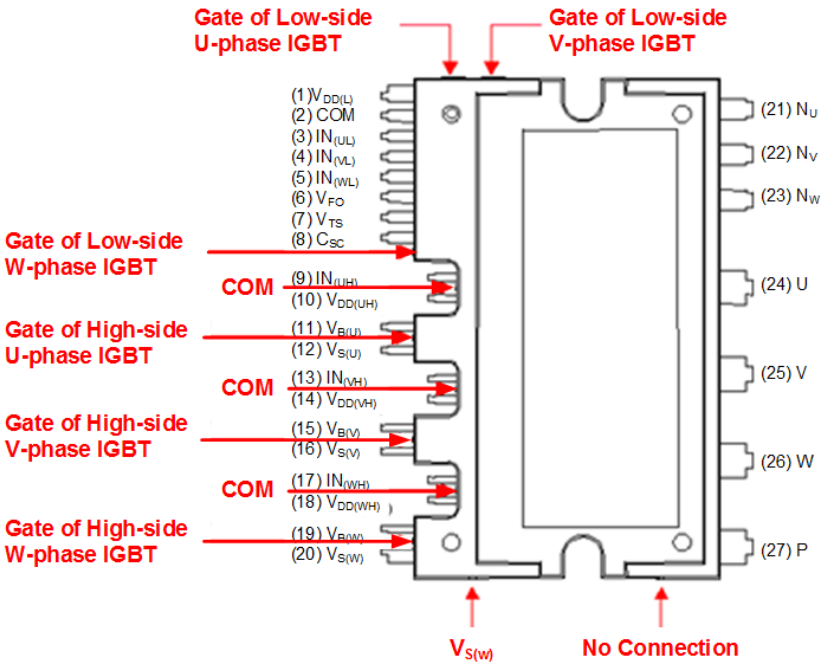


Figure 3. Pin Numbers, Names and Dummy Pins

In the later section illustrates the internal structure of the module in more detail. The detail functional descriptions are provided in Table 3.

Table 3. PIN DEFINITIONS

Pin Number	Name	Description
1	$V_{DD(L)}$	Low−Side Bias Voltage for IC and IGBT Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low−Side U Phase
4	$IN_{(VL)}$	Signal Input for Low−Side V Phase
5	$IN_{(WL)}$	Signal Input for Low−Side W Phase
6	V_{FO}	Fault Output
7	V_{TS}	Output for LVIC Temperature Sensing Voltage
8	C_{SC}	Shunt down input for over current protection
9	$IN_{(UH)}$	Signal Input for High−Side U Phase
10	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBT Driving
11	$V_{B(U)}$	High−Side Bias Voltage for U Phase IGBT Driving
12	$V_{S(U)}$	High−Side Bias Voltage Ground for U Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High−Side V Phase
14	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBT Driving
15	$V_{B(V)}$	High−Side Bias Voltage for V Phase IGBT Driving
16	$V_{S(V)}$	High−Side Bias Voltage Ground for V Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High−Side W Phase
18	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBT Driving

Table 3. PIN DEFINITIONS (continued)

Pin Number	Name	Description
19	$V_{B(W)}$	High−Side Bias Voltage for W Phase IGBT Driving
20	$V_{S(W)}$	High−Side Bias Voltage Ground for W Phase IGBT Driving
21	N_U	Negative DC Link Input for U Phase
22	N_V	Negative DC Link Input for V Phase
23	N_W	Negative DC Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC Link Input

Detailed Pin Definition and Notification

Pins: $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$

- High−side bias voltage pins for driving the IGBT / high−side bias voltage ground pins for driving the IGBTs.
- These are drive power supply pins for providing gate drive power to the high−side IGBTs.
- The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high−side IGBTs.
- Each bootstrap capacitor is charged from the V_{DD} supply during ON state of the corresponding low−side IGBT.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.
- Low−side bias voltage pin / high−side bias voltage pins.

Pins: $V_{DD(L)}$, $V_{DD(H)}$

- These are control supply pins for the built−in ICs.
- These four pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.
- Low−side common supply ground pins.

Pin: COM

- These are supply ground pins for the built−in ICs.
- Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

Pins: $V_{B(U)}$, $V_{B(V)}$, $V_{B(W)}$

- These are pins to connect external bootstrap diode (D_{BS}) for each high−side bootstrapping.
- External resistor (R_{BS}) should be connected between these pins and each VDD.

Pins: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These pins control the operation of the built−in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt−trigger circuit composed of 5 V−class CMOS.
- The signal logic of these pins is active HIGH. The IGBT associated with each of these pins is turned.
- ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the 650V ASPM27 against noise influences.
- To prevent signal oscillations, an RC coupling as illustrated in Figure 37 is recommended.

Pin: C_{SC}

- The current sensing shunt resistor should be connected between the pin C_{SC} and the low−side ground COM to detect short−current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the CSC pin to eliminate noise.
- The connection length between the shunt resistor and CSC pin should be minimized.

Pin: V_{FO}

- Fault output pin.
- This is the fault output alarm pin. An active LOW output is given on this pin for a fault state condition in the ASPM27.
- The alarm conditions are: Short−Circuit Current Protection (SCP), and low−side bias Under−Voltage Lockout (UVLO).
- The VFO output is open drain configured. The VFO signal line should be pulled to the 5 V logic power supply with approximately 4.7kΩ resistance.

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- The VFO output is open drain configured. The VFO signal line should be pulled to the 5 V logic power supply with approximately 4.7kΩ resistance.

Pin: V_{TS}

- This is to indicate the temperature of LVIC with analog voltage. LVIC itself creates some power loss, but mainly heat generated from the IGBTs will increase the temperature of the LVIC.
- VTS versus temperature characteristics is illustrated in Figure 16.
- Analog Temperature Sensing Output Pin**.**
- If don't want use this function, V_{TS} pin should be connected GND with bypass capacitor.

Pin: P

- This is the DC−link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high−side IGBTs.
- To suppress surge voltage caused by the DC−link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).
- Positive DC−link pin

Pins: NU, NV, NW

- These are the DC−link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low−side IGBT emitters of the each phase.
- These pins have to be connected shunt resistor (one or three) for current sensing.
- Inverter power output pins.
- Negative DC−link pins.

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e.g. motor).

Package Structure

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade−off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In 650 V ASPM27, technology was developed with DBC substrate that resulted in good heat dissipation characteristics. Power chips are attached directly to the DBC substrate. This technology is applied 650 V ASPM27, achieving improved reliability and heat dissipation.

Figure 4 shows detail dimensions of the 650 V ASPM27 package. If need more detail data, please refer to the AN−9086.

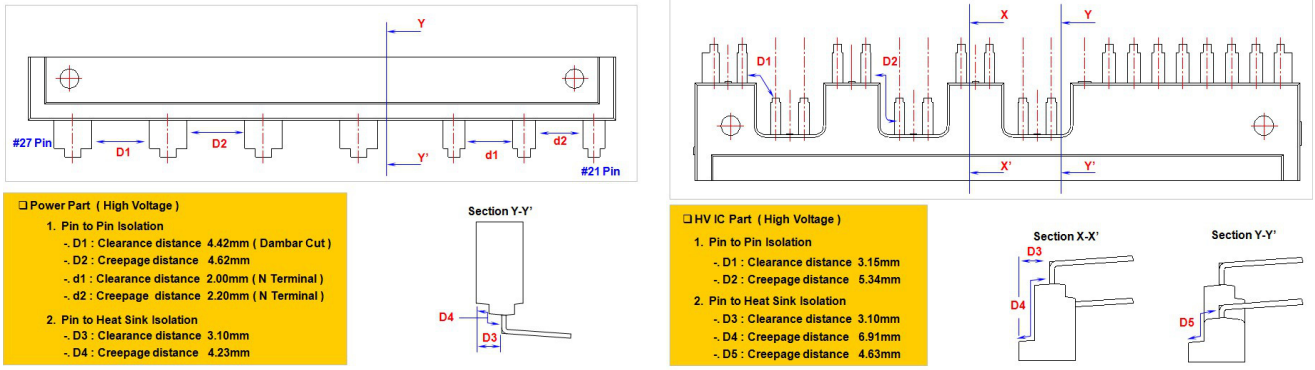


Figure 4. Distance of Isolation for Power Terminal and Control Terminal Part

Figure 5 shows the internal package structure including the lead frame and boding wires. This design has been revise several times to further improve the manufacturability and the reliability to please the customers more.

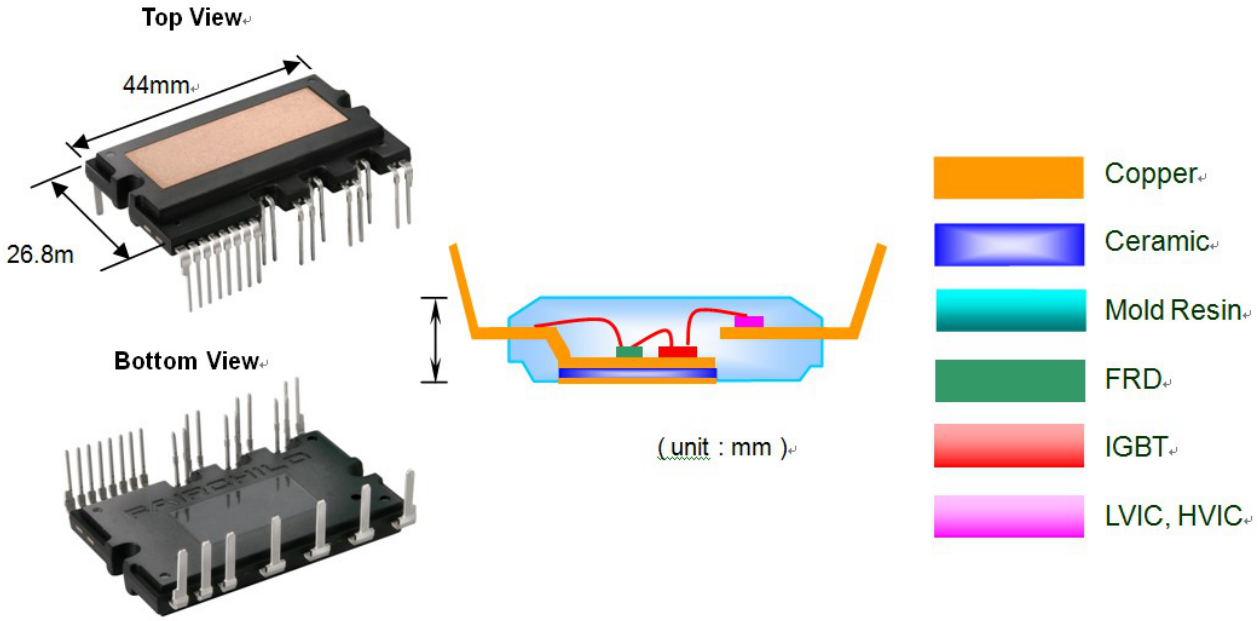
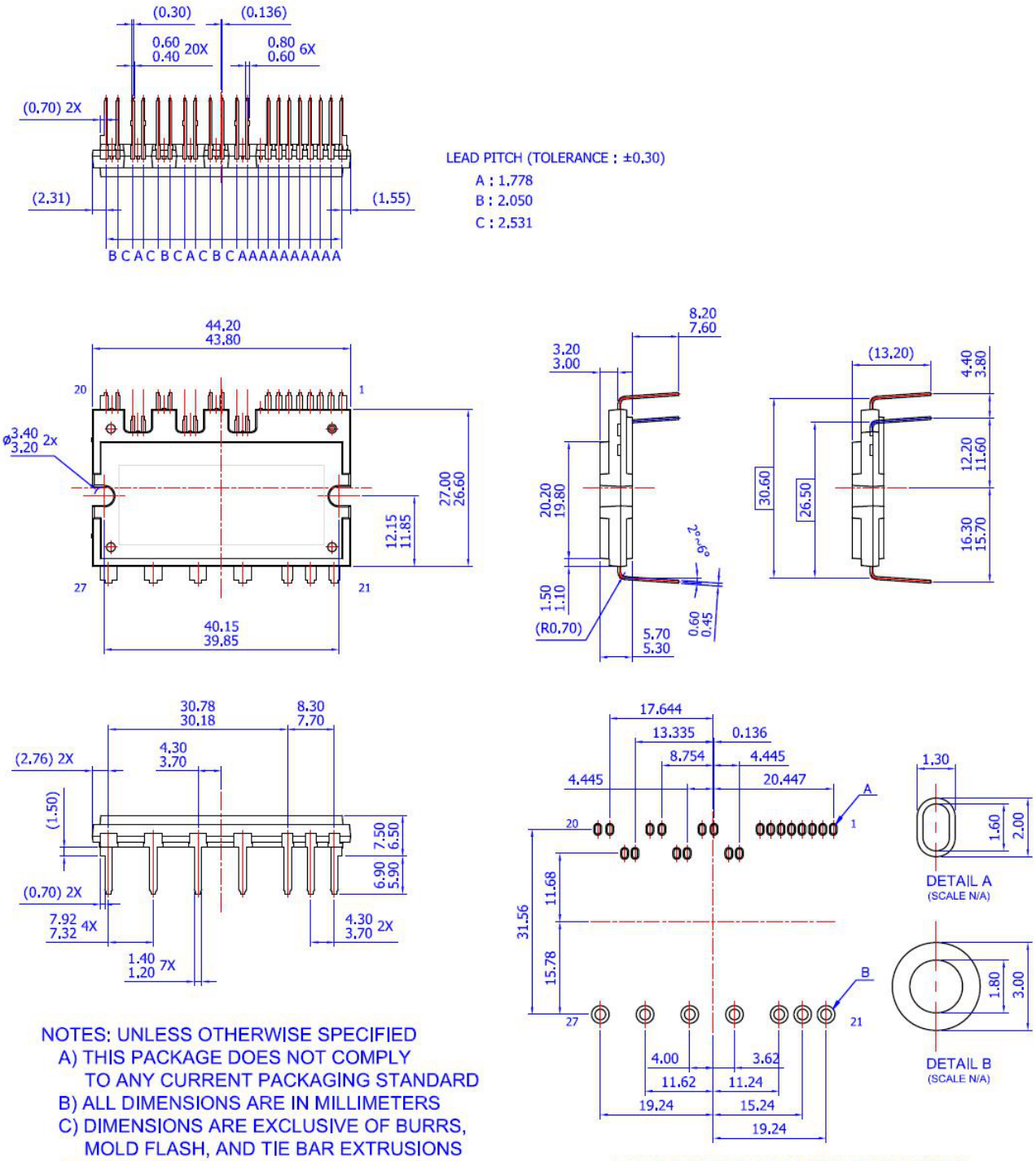


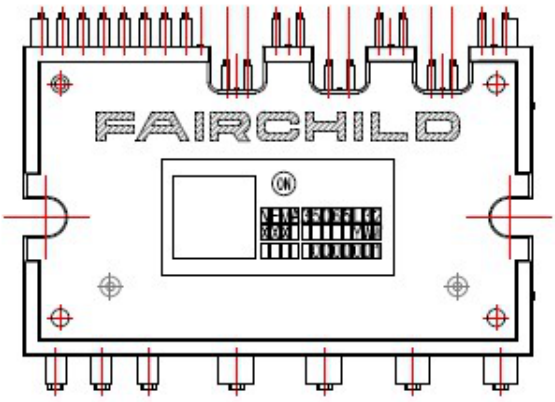
Figure 5. Package Structure and Cross Section for ASPM27

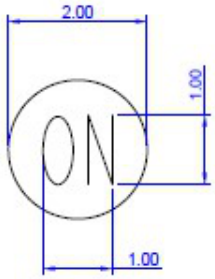
Marking Specification



Marking Specification (continued)

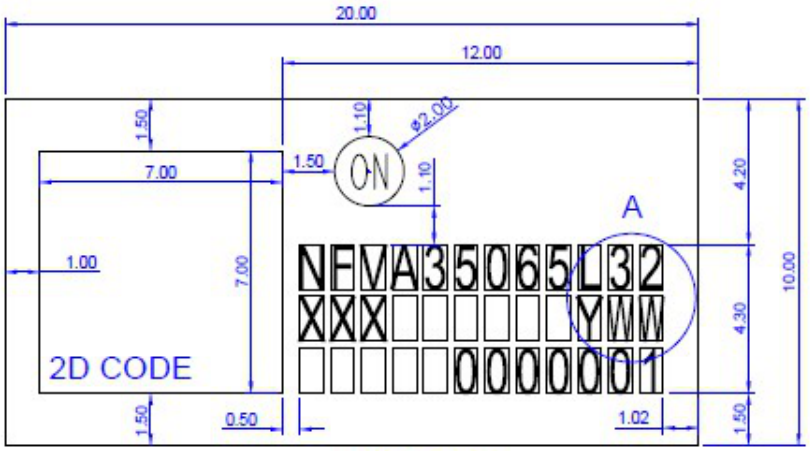
* MARKING LAY-OUT (SCALE 1 : 1)



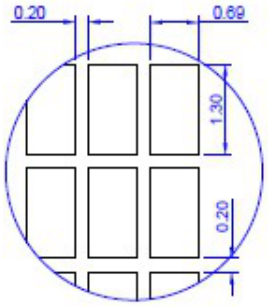


COMPANY LOGO
(SCALE N/A)

* MARKING DIMENSION



(SCALE 3 : 1)



DEATIL A (SCALE 6 : 1)

* 2D CODE

NFVA35065L32xxxH24A0000001

Part Number | Lot Number | Date Code | Marking Machine ID | Serial Number

* NOTE
1. ON : COMPANY LOGO
2. XXX : LAST 3 DIGITS OF LOT NO (OPTION)
3. YWW : DATE CODE (Y : YEAR-SEE THE TABLE, WW : WORK WEEK)
4. 0000001 : SERIAL NUMBER

Y	Alphabet
2017	H
2018	J
2019	K
2020	A
2021	B
2022	C
2023	D
2024	E
2025	F
2026	G
2027	H

PRODUCT SYNOPSIS

This section discusses electrical specification, characteristics and mechanical characteristics.

Absolute Maximum Rating (T_J = 25°C, unless otherwise specified)

Table 4. INVERTER PART (BASE ON NFVA35065L32)

Symbol	Parameter	Conditions	Rating	Unit
V_{PN}	Supply Voltage	Applied between P – NU, NV, NW	500	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P – NU, NV, NW	550	V
V_{CES}	Collector – Emitter Voltage		650	V
$\pm I_C$	Each IGBT Collector Current	T_C = 100°C, $T_{DD} \le$ 15 V, $T_J \le$ 175°C (Note 2)	50	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C = 25°C, $T_J \le$ 175°C, Under 1 ms Pulse Width (Note 3)	100	A
P_C	Collector Dissipation	T_C = 25°C per One Chip	405	W
T_J	Operating Junction Temperature (Note 3)	IGBT and Diode	–40~175	°C
		Driver IC	–40~150	°C

2. There values had been made an acquisition by the calculation considered to design factor.
3. The maximum junction temperature rating of power chips integrated within the 650V ASPM27 products is 175°C.

Table 5. CONTROL PART

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)}$ – COM	20	V
V_{BS}	High–Side Control Bias Voltage	Applied between $V_{B(U)}$–$V_{S(U)}$, $V_{B(V)}$–$V_{S(V)}$, $V_{B(W)}$–$V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM	–0.3~V_{DD}+0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} – COM	–0.3~V_{DD}+0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} – COM	–0.3~V_{DD}+0.3	V

Table 6. TOTAL SYSTEM

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(PROT)}$	Self–Protection Supply Voltage Limit (Short–Circuit Protection Capability)	VDD, VBS = 13.5~16.5 V, T_J = 150°C, Non–Repetitive, < 2 μs	400	V
T_{STG}	Storage Temperature		–55~175	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1–Minute, Connect Pins to Heat Sink	2500	Vrms

Table 7. THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 4)	Inverter IGBT Part (per 1/6 Module)			0.37	°C/W
$R_{th(j-c)F}$		Inverter FWD Part (per 1/6 Module)			1.02	
Lσ	Package Stray Inductance	P to N_U, N_V, N_W (Note 5)		24		nH

4. For the measurement point of case temperature (T_C), please refer Figure 6.
5. Stray inductance per phase measured per IEC 60747–15.

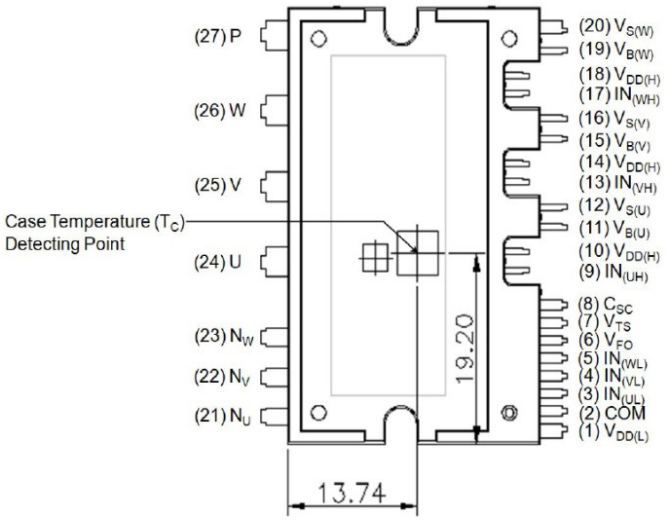


Figure 6. Case Temperature (T_C) Detecting Point

Electrical Characteristic (T_J = 25°C, unless otherwise specified)

Table 8. INVERTER PART (BASE ON NFVA35065L32)

Symbol		Parameter	Condition		Min	Typ	Max	Unit
$V_{CE(SAT)}$		Collector–Emitter Saturation Voltage	V_{DD}, V_{BS}=15 V, V_{IN}=5 V	I_C = 50 A, T_J = 25°C	–	1.70	2.25	V
				I_C = 50 A, T_J = 175°C	–	2.15	2.75	V
V_F		FWDi Forward Voltage	V_{IN} =0 V	I_F = 50 A, T_J = 25°C	–	1.90	2.50	V
				I_F = 50 A, T_J = 175°C	–	1.95	2.55	V
HS	t_{ON}	Switching Times	V_{PN} = 300 V, V_{DD} = 15 V, V_{BS} = 15 V, I_C = 30 A, T_J = 25°C, V_{IN} = 0 V ↔ 5 V, Inductive Load See Figure 7 (Note 6)		0.80	1.20	1.80	μs
	$t_{C(ON)}$				–	0.30	0.75	μs
	t_{OFF}				–	1.25	1.75	μs
	$t_{C(OFF)}$				–	0.15	0.60	μs
	t_{rr}				–	0.15	–	μs
LS	t_{ON}				0.65	1.05	1.65	μs
	$t_{C(ON)}$				–	0.30	0.75	μs
	t_{OFF}				–	1.30	1.80	μs
	$t_{C(OFF)}$				–	0.25	0.60	μs
	t_{rr}				–	0.15	–	μs
I_{CES}		Collector – Emitter Leakage Current	T_J = 25°C, V_{CE} = V_{CES}		–	–	3	mA

6. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detail information, please see and Figure 7.

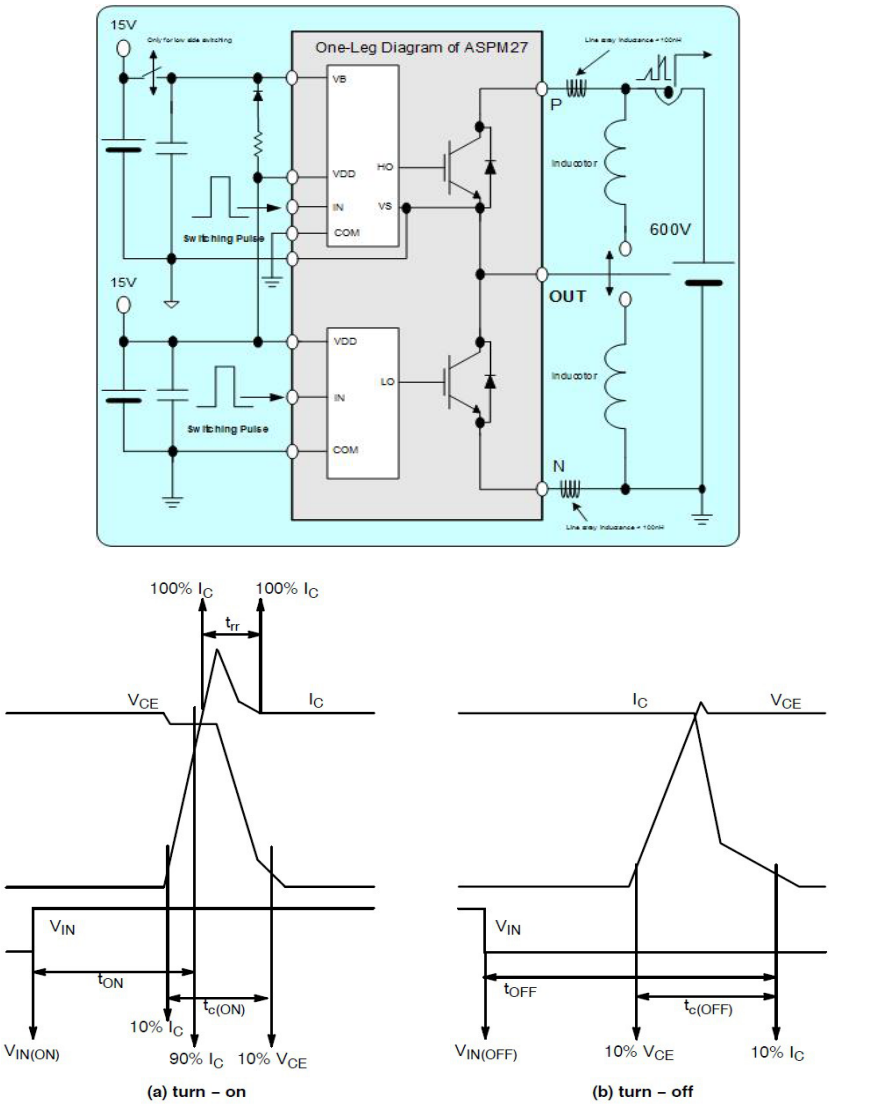


Figure 7. Case Temperature (T_C) Detecting Point

Table 9. CONTROL PART (BASE ON NFVA35065L32)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{QDDH}	Quiescent V_{DD} Supply Current	$V_{DD(H)}$ = 15 V, $IN_{(UH,VH,WH)}$ = 0 V	$V_{DD(H)}$ – COM	–	–	0.40	mA
I_{QDDL}		$V_{DD(L)}$ = 15 V, $IN_{(UL,VL,WL)}$ = 0 V	$V_{DD(L)}$ – COM	–	–	4.80	mA
I_{PDDH}	Operating High−Side V_{DD} Supply Current	$V_{DD(H)}$ = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High Side		–	–	0.48	mA
I_{PDDL}		$V_{DD(L)}$ = 15 V,f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for Low Side		–	–	8.80	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15 V, $IN_{(UH,VH,WH)}$ = 0 V		–	–	0.24	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{DD} = V_{BS} = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High Side		–	–	4.40	mA
V_{FOH}	Fault Output Voltage	V_{DD} = 15 V, V_{SC} = 0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull−up		4.5	–	–	V
V_{FOL}		V_{DD} = 15 V, V_{SC} = 1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull−up		–	–	0.5	V
$V_{SC(ref)}$	Short−Circuit Trip Level	V_{DD} = 15 V (Note 7)	C_{SC} – COM	0.45	0.50	0.55	V

Table 9. CONTROL PART (BASE ON NFVA35065L32) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
UV_{DDD}	Supply Circuit, Under−Voltage Protection	Detection Level	9.80	−	13.3	V
UV_{DDR}		Reset Level	10.3	−	13.8	V
UV_{BSD}		Detection Level	9.00	−	12.5	V
UV_{BSR}		Reset Level	9.50	−	13.0	V
t_{FOD}	Fault−Out Pulse Width		50	−	−	μs
V_{TS}	LVIC Temperature Sensing Voltage Output	$V_{DD(L)}$ = 15 V, T_{LVIC} = 25°C, See Figure 8 (Note 8)	540	640	740	mV
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(UH,VH,WH)}$−COM, $IN_{(UL,VL,WL)}$−COM	−	−	2.60	V
$V_{IN(OFF)}$	OFF Threshold Voltage		0.80	−	−	V

7. Short−circuit current protection is functioning only at the low−sides.
8. T_{LVIC} is the temperature of LVIC itself, V_{TS} is only for sensing temperature of LVIC and cannot shutdown IGBTs automatically.

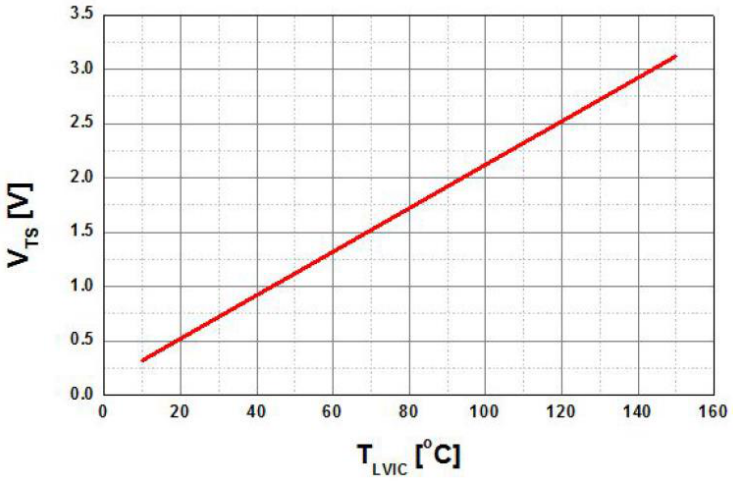


Figure 8. Temperature Profile of V_{TS} (Typical)

Recommended Operating Conditions

Table 10. RECOMMENDED OPERATING CONDITIONS (BASE ON NFVA35065L32)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P−N_U, N_V, N_W	−	300	400	V
V_{DD}	Control Supply Voltage	Applied between $V_{DD(UH,VH,WH)}$−COM, $V_{DD(L)}$−COM	14.0	15.0	16.5	V
V_{BS}	High−Side Bias Voltage	Applied between $V_{B(U)}$−$V_{S(U)}$, $V_{B(V)}$−$V_{S(V)}$, $V_{B(W)}$−$V_{S(W)}$	13.0	15.0	18.5	V
dV_{DD}/dt, dV_{BS}/dt	Control Supply Variation		−1	−	1	V/ms
t_{dead}	Blanking Time for Preventing Arm−Short	For Each Input Signal	2.0	−	−	ms
f_{PWM}	PWM Input Signal	−40°C ≤ T_C ≤ 175°C, −40°C ≤ T_J ≤ 175°C	−	−	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W−COM (Including Surge Voltage)	−5	−	5	V

Table 10. RECOMMENDED OPERATING CONDITIONS (BASE ON NFVA35065L32) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$P_{WIN(ON)}$	Minimum Input Pulse Width	V_{DD} = V_{BS} = 15 V, I_C ≤ 50 A, Wiring Inductance between $N_{U,V,W}$ and DC Link N < 10nH (Note 9)	2.0	–	–	μs
$P_{WIN(OFF)}$			2.0	–	–	–
$P_{WIN(ON)}$		V_{DD} = V_{BS} = 15 V, I_C ≤ 100A, Wiring Inductance between $N_{U,V,W}$ and DC Link N < 10nH (Note 9)	2.5	–	–	μs
$P_{WIN(OFF)}$			2.5	–	–	–
T_J	Junction Temperature		–40	–	150	°C

9. This product might not make response if input pulse with is lee than the recommended value.

Mechanical Characteristics

Table 11. MECHANICAL CHARACTERISTICS

Parameter	Condition		Min	Typ	Max	Unit
Device Flatness	See Figure 9		0	–	+150	μm
Mounting Torque	Mounting Screw: M3 See Figure 10	Recommended 0.7 N•m	0.6	0.7	0.8	N•m
		Recommended 7.1 kg•cm	6.2	7.1	8.1	kg•cm
Terminal Pulling Strength	Load 19.6 N		10	–	–	s
Terminal Bending Strength	Load 9.8 N, 90° Bend		2	–	–	Times
Weight	Module Weight		–	15	–	g

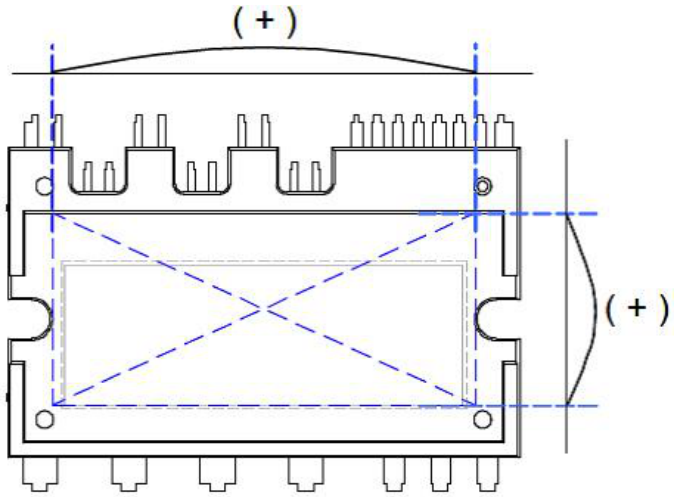
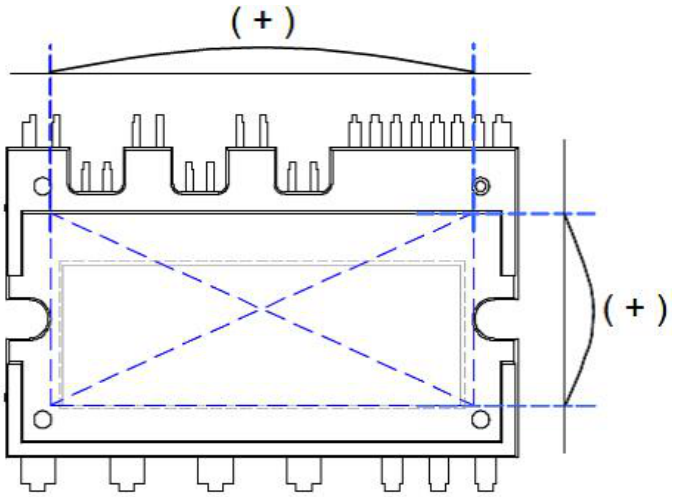


Figure 9. Flatness Measurements Position



NOTES: Do not make over torque when mounting screws. Much mounting torque may cause DBC crack, as well as bolts Al heat sink destruction.
Avoid one−sided tightening stress, Figure 10 shows the recommended torque order for mounting order for mounting screws. Uneven mounting can cause the DBC substrate of package to be damaged. The pre−screwing torque is set to 20~30% of maximum torque rating.

Figure 10. Flatness Measurements Position

OPERATION SEQUENCE FOR PROTECTIONS

Short Circuit Protection

The 650 V ASPM27 uses external shunt resistor for the short circuit current detection, as shown in Figure 11. The LVIC has a built−in short−circuit current protection function. This protection function senses the voltage to the CSC pin. If this voltage exceeds the $V_{SC(ref)}$ (the threshold voltage trip level of the short−circuit) specified in the device datasheets ($V_{SC(ref)}$, typ. is 0.5 V), a fault signal is asserted and the all low side IGBTs are turned off.

Typically, the maximum short−circuit current magnitude is gate−voltage dependent: higher gate voltage (V_{DD} and V_{BS}) results in larger short−circuit current. To avoid potential problems, the maximum short−circuit trip level is set below 1.5 times the nominal rated collector current. The LVIC short−circuit current protection−timing chart is shown in Figure 12.

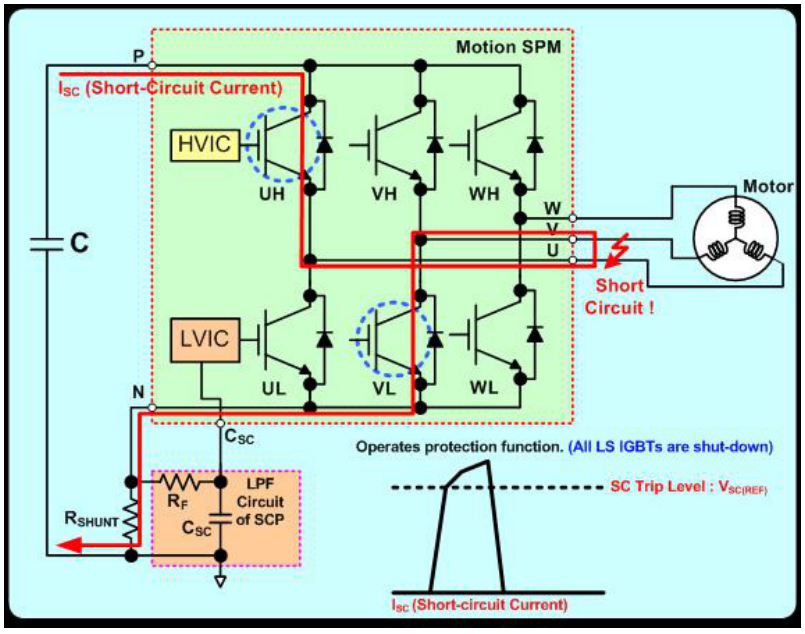
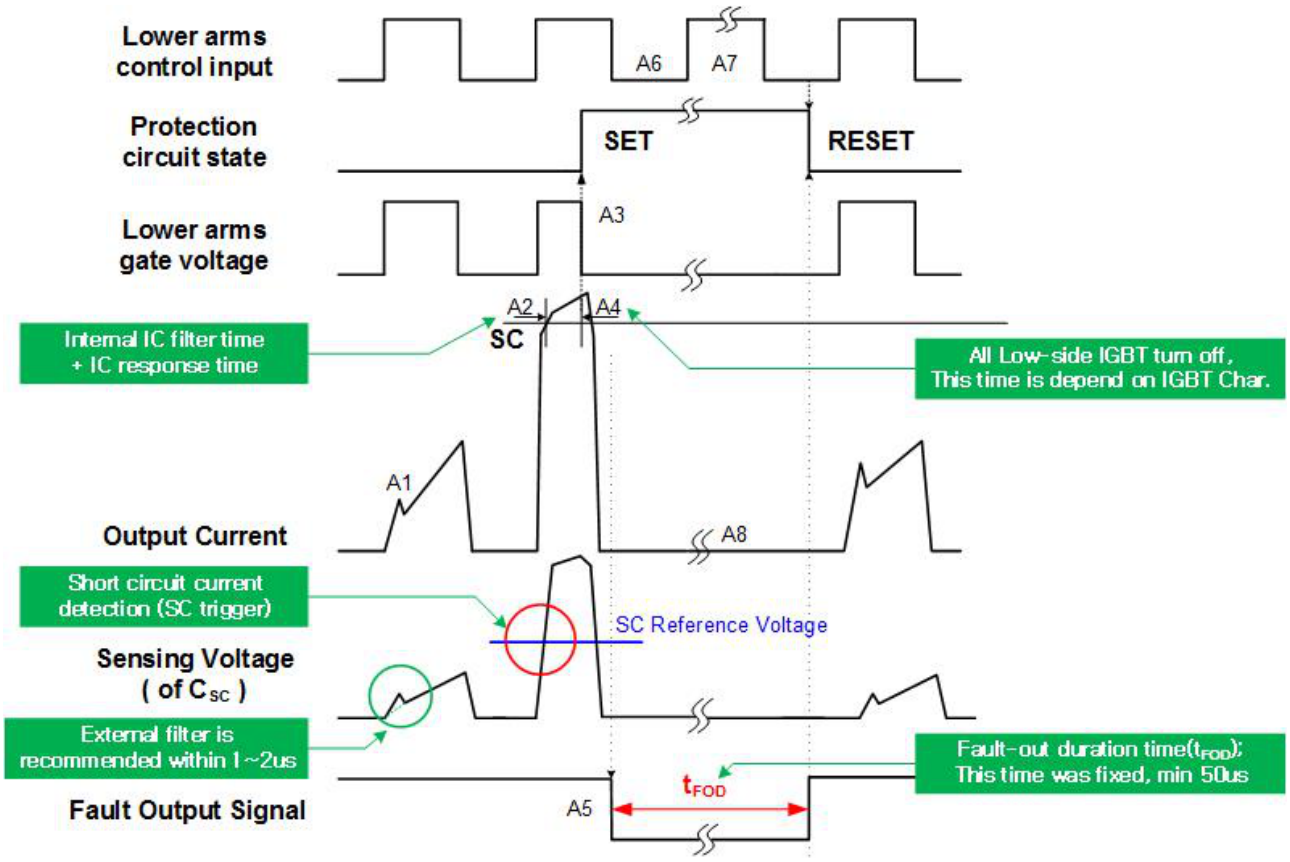


Figure 11. Operation of Short−Circuit Protection

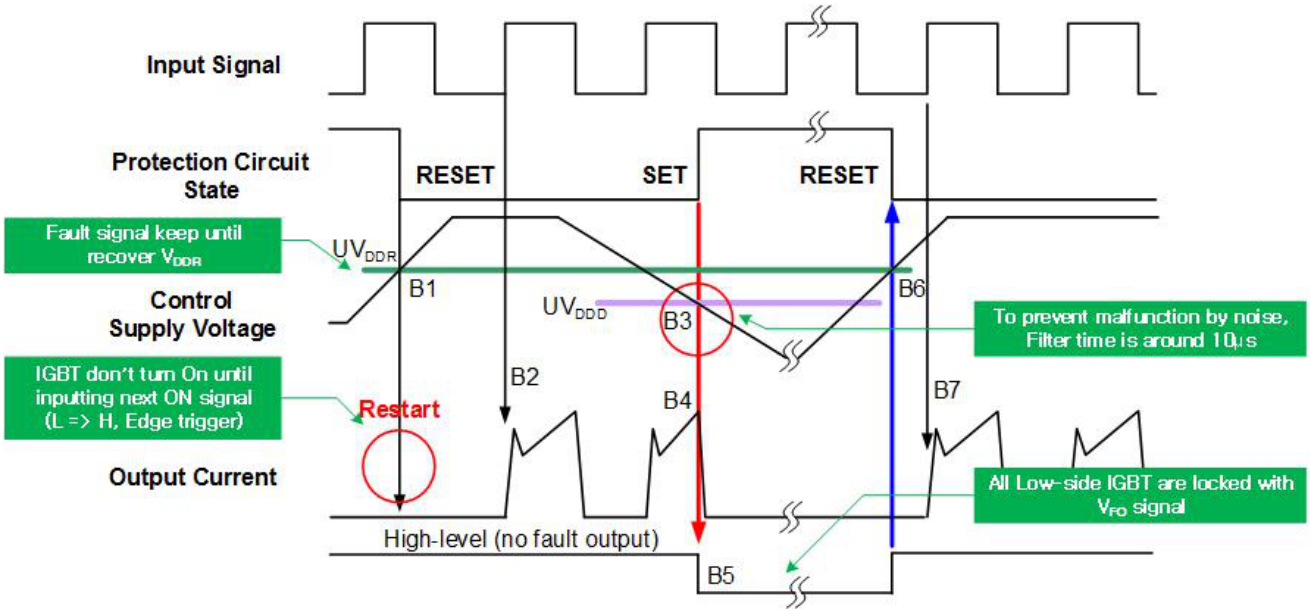


NOTES: A1– normal operation: IGBT on and carrying current
A2 – short–circuit current detection (SC trigger)
A3 – hard IGBT gate interrupt
A4 – IGBT turns OFF
A5 – fault output timer operation start with internal delay (typ. 2.8 μs), Fault–out duration time is fix (min. 50 μs)
A6 – input “L”: IGBT OFF state
A7 – input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON
A8 – IGBT keeps OFF state

Figure 12. Timing Chart of Short–Circuit Protection Function

Under−Voltage Lockout Protection (Low−side UVLO)

The LVIC has an Under−Voltage Lockout protection (UVLO) function to protect the low−side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 13.

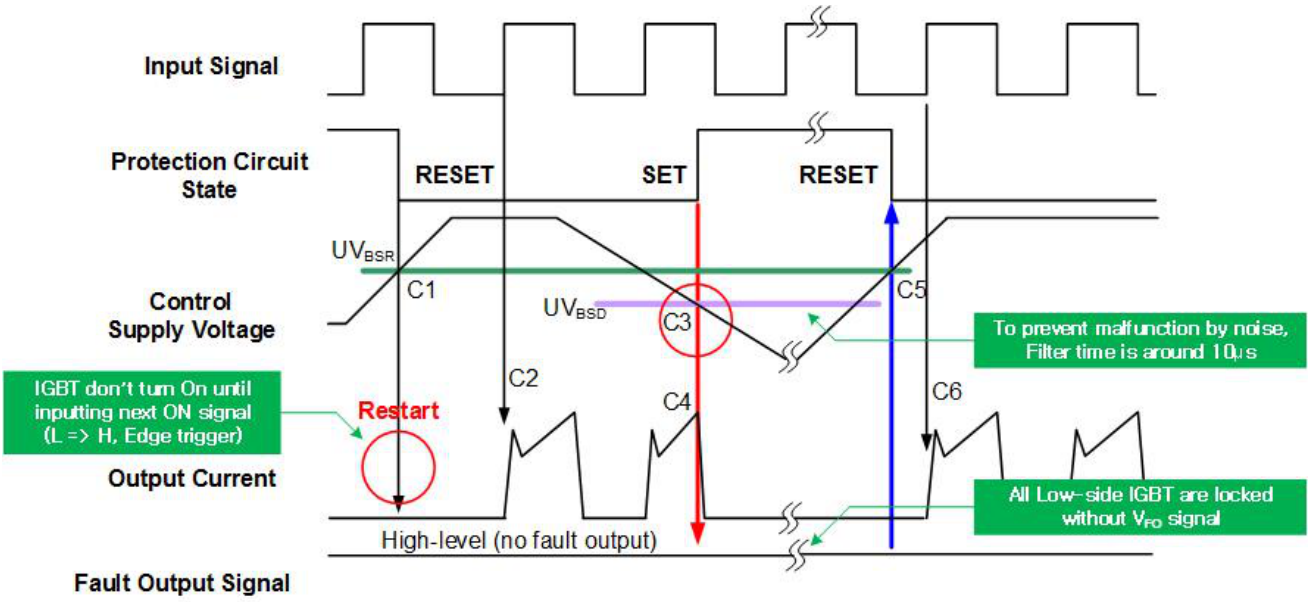


NOTES: B1− control supply voltage rise: after the voltage rises UV_{DDR}, the circuits starts to operate when the next input is applied (L => H)
B2 − normal operation: IGBT ON and carrying current
B3 − under−voltage detection (UV_{DDD})
B4 − IGBT OFF in spite of control input is alive
B5 − Fault output signal starts
B6 − under−voltage reset (UV_{DDR})
B7 − normal operation: IGBT ON and carrying current

Figure 13. Timing Chart of Low−side Under−Voltage Protection Function

Under−Voltage Lockout Protection (High−side UVLO)

The HVIC has an under−voltage lockout function to protect the high−side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 14. The fault−out (FO) alarm is not given for low HVIC bias conditions.



NOTES: C1− control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts when the next input is applied)
C2 − normal operation: IGBT ON and carrying current
C3 − under−voltage detection (UV_{BSD})
C4 − IGBT OFF in spite of control input is alive, but there is no fault output signal
C5 − under−voltage reset (UV_{BSR})
C6 − normal operation: IGBT ON and carrying current

Figure 14. Timing Chart of High−side Under−Voltage Protection Function

KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the 650 V ASPM27.

Thermal Sensing Unit (TSU)

The junction temperature of power devices should not exceed the maximum junction temperature. Even though there is some margin between the T_{JMAX} specified on the datasheet and the actual T_{JMAX} at which power devices get destroyed, caution should be given to make sure the junction temperature stays well below the T_{JMAX}.

Basic Concept

Thermal Sensing Unit uses technology based on the temperature dependency of transistor Vbe; Vbe decrease 2 mV as temperature increase 1°C.

The Thermal Sensing Unit analog voltage output reflects the temperature of the LVIC in 650 V ASPM27 series products. The relationship between V_{TS} voltage output and LVIC temperature is shown in Figure 16. It does not have any self−protection function, and, therefore, it should be used appropriately based on application requirement. It should be noted that there is a time lag from IGBT temperature to LVIC temperature. It is very difficult to respond quickly when temperature rises sharply in a transient condition such as shoot−through event. Even though TSU has some limitation, it will be definitely useful in enhancing the system reliability.

Figure 15 shows the LVIC location of ASPM27 series.

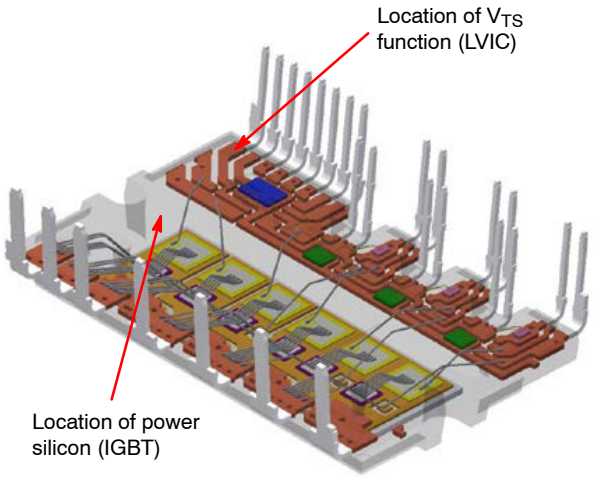


Figure 15. Location of VTS Function (LVIC)

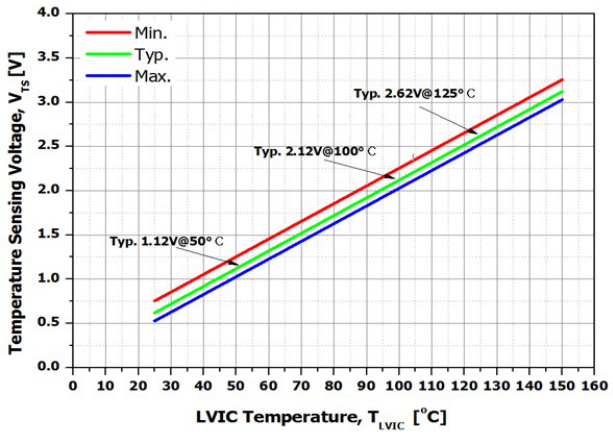


Figure 16. Temperature vs. V_{TS}

Figure 17 shows the equivalent circuit diagram of V_{TS} inside IC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal Zener diode, but in case the maximum input range of Analog to Digital converter of MCU is below 5.2 V, an external Zener diode should be inserted between an A/D input pin and the analog ground pin of MCU. An amplifier can be used to change the range of voltage input to the Analog to Digital converter to have better resolution of the temperature. It is recommended to add a ceramic capacitor of 1000 pF between V_{TS} and Com (Ground) to make the V_{TS} more stable. If don't use this function, customer have to connect a ceramic capacitor of 1000 pF between V_{TS} and Com (Ground) because this V_{TS} pin is live voltage output pin.

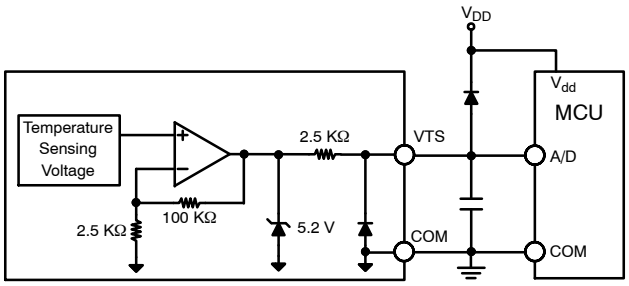


Figure 17. Internal Block Diagram and Interface Circuit of TSU

Figure 18 shows the sourcing capability of V_{TS} pin at 25°C and the test method. V_{TS} voltage decreases as the sourcing current increases. Therefore, the load connected to V_{TS} pin should be minimized to maintain the accurate voltage output level without degradation. Figure 16 shows that the relationship between V_{TS} voltage and LVIC temperature. It can be expressed as the following equation.

- $V_{TS.min} = 0.02 \times T_{LVIC} + 0.04$ [V]
- $V_{TS.typ} = 0.02 \times T_{LVIC} + 0.14$ [V]
- $V_{TS.max} = 0.02 \times T_{LVIC} + 0.24$ [V]

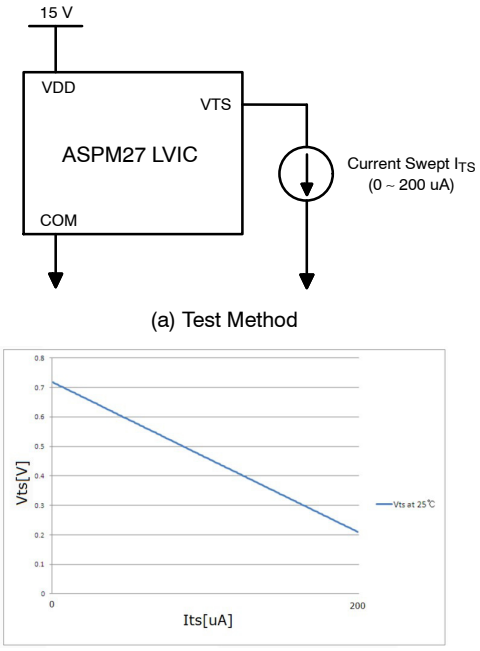


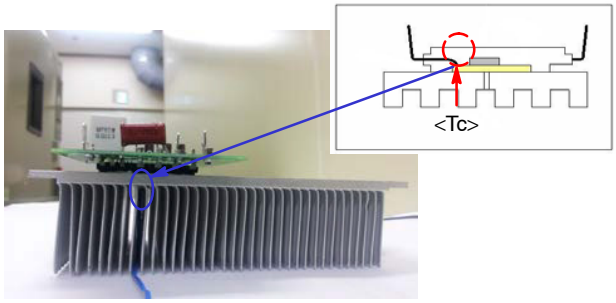
Figure 18. Real Load Variation of VTS

The maximum variation of V_{TS} is 0.24 V, and the minimum variation of V_{TS} is 0.04 V due to process variation which is equivalent ±5°C approximately. This is regardless of the temperature because the slopes of three lines are identical. If the ambient temperature information is available, for example, through NTC in the system, V_{TS} can be measured to adjust the offset before the motor starts to operate.

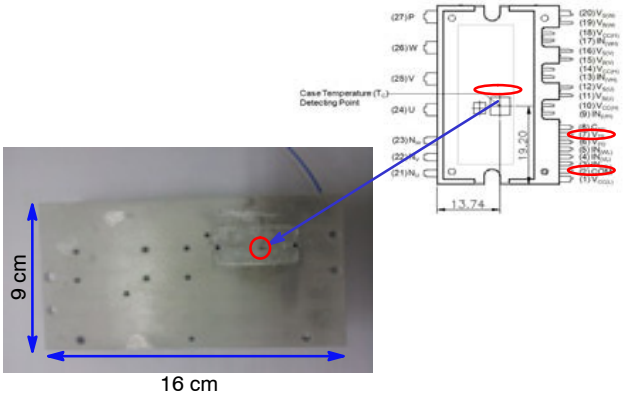
As temperature decreases further below 0°C, V_{TS} decreases linearly until it reaches zero volts. If the temperature of LVIC increases above 150ºC, which is above the maximum operating temperature, V_{TS} would increase theoretically up to 5.2 V until it gets clamped by the internal Zener diode.

Test Method

This test result shows correlation between V_{TS} and T_C, but this correlation will be changed each customer real application conditions. Figure 19 shows the test board and temperature measure point.



(a) Test Board



(b) Heat−Sink Size and Measure Point of T_C

Figure 19. Heat−Sink Size and Measure Point of T_C

We tested real load by servo dynamo systems, refer to the Figure 20.

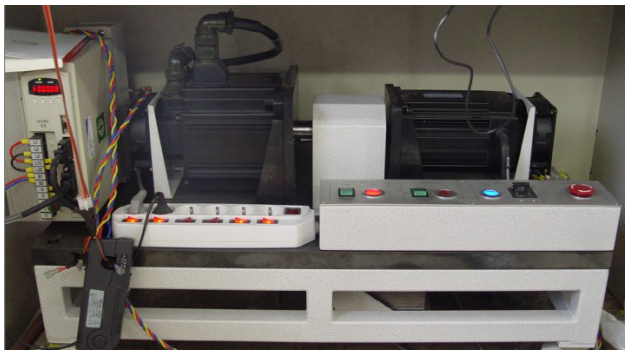


Figure 20. Real Load Dynamo System

We have compared between convection cooling and forced cooling mode. Figure 21 shows the cooling conditions.

To avoid external environment, we used the case, refer to Figure 22.

Test conditions were V_{DD} = 15 V, V_{DC} = 300 V, Frequency = 5 kHz and PWM method = SPWM.

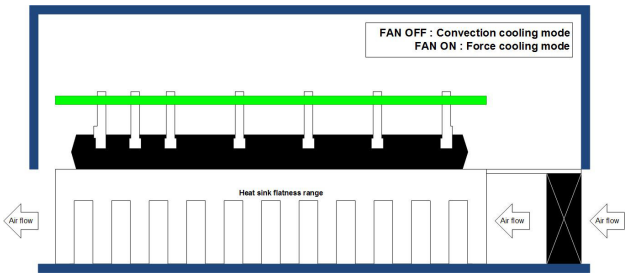


Figure 21. Cooling Conditions

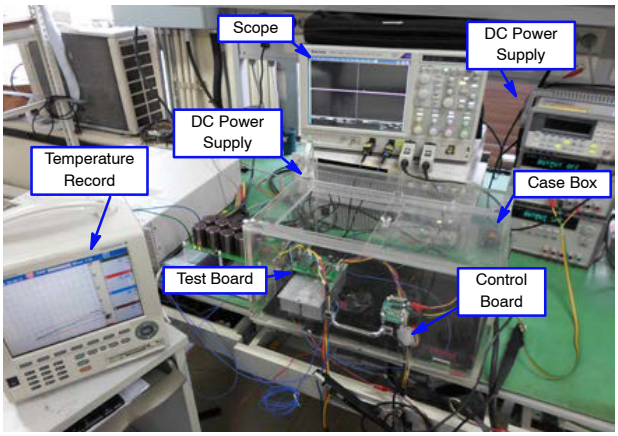


Figure 22. Test Environment

Test Results

Figure 23 and Figure 24 shows the test result. As the test results, T_C and V_{TS} temperatures have a variable gap by cooling conditions. Fragmentarily, this test result shows, V_{TS} value is depend on cooling conditions (Heat sink size, Fan speed and etc). Temperature gap has about 20 degree between T_C and V_{TS} in convection cooling mode. And gap has about 10 degree in force cooling mode.

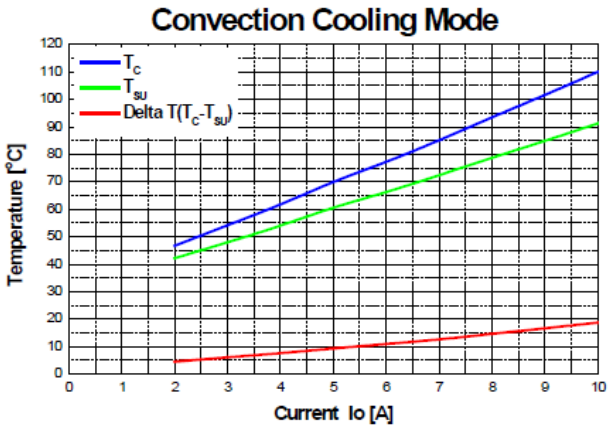


Figure 23. Convection Cooling Mode

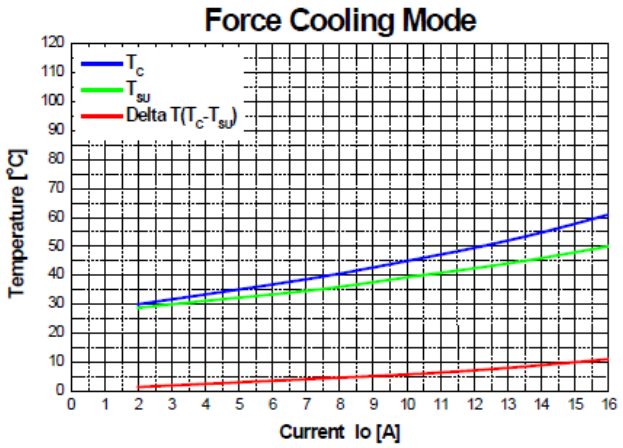


Figure 24. Force Cooling Mode

In conclusion, if the customers want to use the thermal sensing unit (T_{SU}), they should make adjustment in real operation conditions by themselves. And heat generated at IGBT and FWDi transfer to LVIC through modeling resin of package and outer heat sink. So LVIC temperature cannot respond to rapid temperature rise of those power chips effectively.

Table 12. V_{TS} TABLE OF LVIC

T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)	T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)
25	0.54	0.64	0.74	88	1.80	1.90	2.00
26	0.56	0.66	0.76	89	1.82	1.92	2.02
27	0.58	0.68	0.78	90	1.84	1.94	2.04
28	0.60	0.70	0.80	91	1.86	1.96	2.06
29	0.62	0.72	0.82	92	1.88	1.98	2.08
30	0.64	0.74	0.84	93	1.90	2.00	2.10
31	0.66	0.76	0.86	94	1.92	2.02	2.12
32	0.68	0.78	0.88	95	1.94	2.04	2.14
33	0.70	0.80	0.90	96	1.96	2.06	2.16
34	0.72	0.82	0.92	97	1.98	2.08	2.18
35	0.74	0.84	0.94	98	2.00	2.10	2.20
36	0.76	0.86	0.96	99	2.02	2.12	2.22
37	0.78	0.88	0.98	100	2.04	2.14	2.24
38	0.80	0.90	1.00	101	2.06	2.16	2.26
39	0.82	0.92	1.02	102	2.08	2.18	2.28
40	0.84	0.94	1.04	103	2.10	2.20	2.30
41	0.86	0.96	1.06	104	2.12	2.22	2.32
42	0.88	0.98	1.08	105	2.14	2.24	2.34
43	0.90	1.00	1.10	106	2.16	2.26	2.36
44	0.92	1.02	1.12	107	2.18	2.28	2.38
45	0.94	1.04	1.14	108	2.20	2.30	2.40
46	0.96	1.06	1.16	109	2.22	2.32	2.42
47	0.98	1.08	1.18	110	2.24	2.34	2.44
48	1.00	1.10	1.20	111	2.26	2.36	2.46
49	1.02	1.12	1.22	112	2.28	2.38	2.48
50	1.04	1.14	1.24	113	2.30	2.40	2.50
51	1.06	1.16	1.26	114	2.32	2.42	2.52
52	1.08	1.18	1.28	115	2.34	2.44	2.54
53	1.10	1.20	1.30	116	2.36	2.46	2.56

Table 12. V_{TS} TABLE OF LVIC (continued)

T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)	T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)
54	1.12	1.22	1.32	117	2.38	2.48	2.58
55	1.14	1.24	1.34	118	2.40	2.50	2.60
56	1.16	1.26	1.36	119	2.42	2.52	2.62
57	1.18	1.28	1.38	120	2.44	2.54	2.64
58	1.20	1.30	1.40	121	2.46	2.56	2.66
59	1.22	1.32	1.42	122	2.48	2.58	2.68
60	1.24	1.34	1.44	123	2.50	2.60	2.70
61	1.26	1.36	1.46	124	2.52	2.62	2.72
62	1.28	1.38	1.48	125	2.54	2.64	2.74
63	1.30	1.40	1.50	126	2.56	2.66	2.76
64	1.32	1.42	1.52	127	2.58	2.68	2.78
65	1.34	1.44	1.54	128	2.60	2.70	2.80
66	1.36	1.46	1.56	129	2.62	2.72	2.82
67	1.38	1.48	1.58	130	2.64	2.74	2.84
68	1.40	1.50	1.60	131	2.66	2.76	2.86
69	1.42	1.52	1.62	132	2.68	2.78	2.88
70	1.44	1.54	1.64	133	2.70	2.80	2.90
71	1.46	1.56	1.66	134	2.72	2.82	2.92
72	1.48	1.58	1.68	135	2.74	2.84	2.94
73	1.50	1.60	1.70	136	2.76	2.86	2.96
74	1.52	1.62	1.72	137	2.78	2.88	2.98
75	1.54	1.64	1.74	138	2.80	2.90	3.00
76	1.56	1.66	1.76	139	2.82	2.92	3.02
77	1.58	1.68	1.78	140	2.84	2.94	3.04
78	1.60	1.70	1.80	141	2.86	2.96	3.06
79	1.62	1.72	1.82	142	2.88	2.98	3.08
80	1.64	1.74	1.84	143	2.90	3.00	3.10
81	1.66	1.76	1.86	144	2.92	3.02	3.12
82	1.68	1.78	1.88	145	2.94	3.04	3.14
83	1.70	1.80	1.90	146	2.96	3.06	3.16
84	1.72	1.82	1.92	147	2.98	3.08	3.18
85	1.74	1.84	1.94	148	3.00	3.10	3.20
86	1.76	1.86	1.96	149	3.02	3.12	3.22
87	1.78	1.88	1.98	150	3.04	3.14	3.24

Selection of Shunt Resistor

Figure 25 shows an example circuit of the SC protection using 1−shunt resistor. The line current on the N side DC−ink is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N−side three−phase IGBTs are switched to the OFF state and the F_O fault signal is transmitted to MCU. Since SC protection is non−repetitive, IGBT operation should be immediately halted when the F_O fault signal is given.

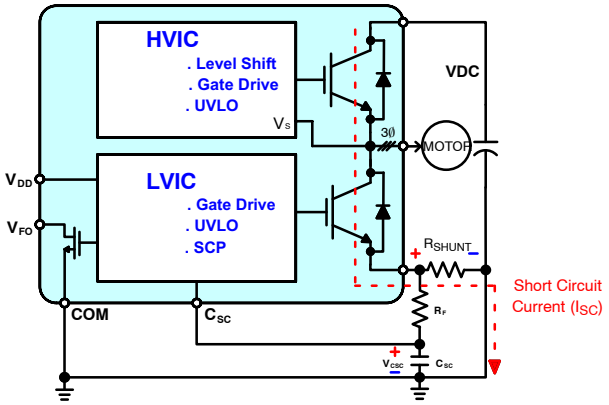


Figure 25. Short Circuit Current Protection Circuit with One Shunt Resistor

The value of shunt resistor is calculated by the following equation

- Maximum SC current trip level:
  $I_{SC(max)}$=1.5 × I_C (rated current)
- SC trip referenced voltage: V_{SC} = min. 0.45 V, typ. 0.5 V, max. 0.55 V
- Shunt resistance: $I_{SC(max)} = V_{SC(max)}/R_{SHUNT(min)}$ → $R_{SHUNT(min)} = V_{SC(max)}/I_{SC(max)}$
- If the deviation of shunt resistor should is limited below ±5%, $R_{SHUNT(typ)} = R_{SHUNT(min)}/0.95$, $R_{SHUNT(max)} = R_{SHUNT(typ)} \times 1.05$
- Actual SC trip current level becomes:
  $I_{SC(typ)} = V_{SC(typ)}/R_{SHUNT(min)}$,
  $I_{SC(min)} = V_{SC(min)}/R_{SHUNT(max)}$
- Inverter output power:

$$Pout = \sqrt{3} \times VO, LL \times I_{O(RMS)} \times PF$$

Where:

$$VO, LL = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC}}{2}$$

I(O)RMS = Maximum load current of inverter; and
MI = Modulation Index
VDC = DC link voltage
PF = Power Factor

- Average DC Current
  $I_{DC\_AVG} = V_{DC\_Link} / (P_{out} \times Eff)$
  Where:
  Eff = Inverter Efficiency
- The power rating of shunt resistor is calculated by the following equation.
  $P_{SHUNT} = (I^2_{RMS} \times R_{SHUNT} \times Margin)/De-rating\ Ratio$
  Where:
  Shunt resistor typical value at T_C = 25°C (R_{SHUNT})
  De−rating ratio of shunt resistor at T_{SHUNT}=100°C (From datasheet of shunt resistor)
  Safety margin (Determine by customer)

The value of shunt resistor calculation examples

- DUT: NFVA33065L32
- Tolerance of shunt resistor: ±5%
- SC Trip Reference Voltage:
  $V_{SC(min)}$ = 0.45 V, $V_{SC(typ)}$ = 0.50 V, $V_{SC(max)}$ = 0.55 V
- Maximum Load Current of Inverter (I_{RMS}): 21 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{C(max)}$): 45 A
- Modulation Index(MI): 0.9
- DC Link Voltage(V_{DC_Link}): 300 V
- Power Factor (PF): 0.8
- Inverter Efficiency(Eff): 0.95
- Shunt Resistor Value at T_C = 25°C (R_{SHUNT}): 11.0 mΩ
- De−rating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70% (refer to Figure 28)
- Safety Margin: 20%

Calculation results

- $I_{SC(max)}$: 1.5 × $I_{C(max)}$ = 1.5 × 30 A = 45 A
- $R_{SHUNT(typ)}$: $V_{SC(typ)}$ / $I_{SC(max)}$ = 0.50 V/45 A = 11.0 mΩ
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)}$ × 1.05 = 11 mΩ × 1.05 A = 11.55 mΩ
- $R_{SHUNT(min)}$: $R_{SHUNT(typ)}$ × 0.95 = 11 mΩ × 0.95 A = 10.45 mΩ
- $I_{SC(min)}$: $V_{SC(min)}/R_{SHUNT(max)}$ = 0.45 V/11.55 mΩ = 38.96 A
- $I_{SC(max)}$: $V_{SC(typ)}/R_{SHUNT(min)}$ = 0.55 V/10.45 mΩ = 52.6 A
- $$Pout = \sqrt{3} \times (\frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC}}{2}) \times I_{(0)RMS} \times PF$$
  $$= \frac{3}{\sqrt{2}} \times 0.9 \times (\frac{300}{2}) \times 21 \times 0.8 = 4.811W$$
- I_{DC_AVG} = (P_{OUT}/Eff) / V_{DC_Link} = 16.88 A
- P_{SHUNT} = ($I^2_{DC\_AVG} \times R_{SHUNT} \times Margin$)/De−rating Ratio = ($16.88^2 \times 0.012 \times 1.2$) / 0.7 = 5.86 W (therefore, the proper power rating of shunt resistor is over 6.0 W)

When over−current events are detected, the 650 V ASPM27 series shuts down all low−side IGBTs and sends out the fault−out (F_O) signal. Fault−out pulse width is fixed; minimum value is 50 μs.

To prevent malfunction, it is recommended that an RC filter be inserted at the C_{SC} pin. To shut down IGBTs within 3 μs when over−current situation occurs, a time constant of 1.5~2 μs is recommended. Table 13 shows the shunt resistance and typical short−circuit protection current.

Table 13. OVER−CURRENT (OC) PROTECTION TRIP LEVEL

Device	R_{SHUNT}	OC Trip Level	Remark
NFVA33065L32	11 mΩ	45 A	It is typical value
NFVA34065L32	8.3 mΩ	60 A	
NFVA35065L32	6.7 mΩ	75 A	

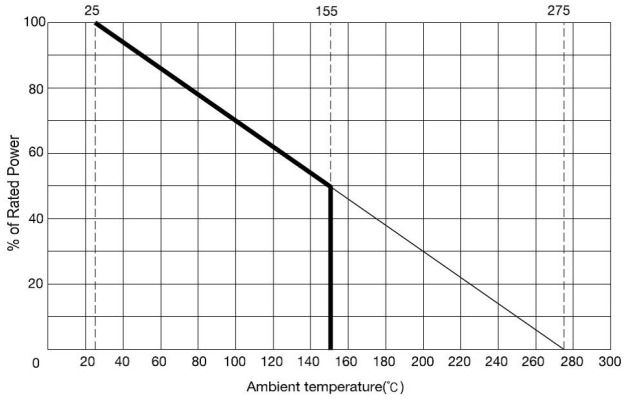
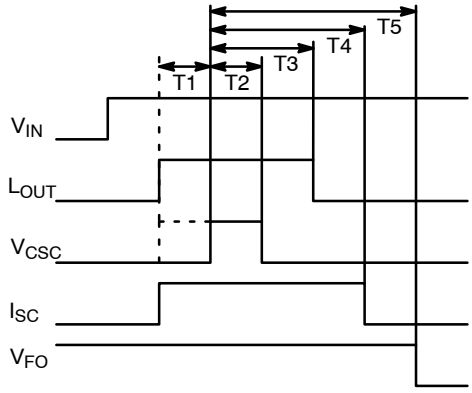


Figure 26. De−rating Curve Example of Shunt Resistor (from RARA Elec.)

Time Constant of Internal Delay

An RC filter is prevents noise−related Short−Circuit Current Protection (SCP) circuit malfunction. The RC time constant is determined by the applied noise time and the Short−Circuit Current Withstanding Time (SCWT) of ASPM27 series.

When the R_{SC} voltage exceeds the SCP level, this is applied to the CSC pin via the RC filter. The RC filter delay (T1) is the time required for the CSC pin voltage to rise to the referenced SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: T2, around 0.7 μs). Consider this filter time when designing the RC filter of V_{CSC}.



NOTES: V_{IN}: Voltage of input signal
LOUT: VGE of low−side IGBT
VCSC: Voltage of CSC pin
ISC: Short−circuit current
VFO: Voltage of VFO pin
T1: filtering time of RC filter of VCSC
T2: filtering time of CSC. If VCSC width is less than T2, SCP does not operate
T3: delay from CSC triggering to gate−voltage down
T4: delay from CSC triggering to short−circuit current
T5: delay from CSC triggering to fault−out signal

Figure 27. Timing Diagram

Figure 28 shows operating waveform of SCP (Short−circuit Current Protection) function. Normally, **t**(time constant of RC filter of C_{SC}) don't accurately operate due to fast di/dt of I_{SC} (short−circuit current). Therefore, we should consider this kind of situation when decide time constant of RC filter of C_{SC}. Normally, T (time constant of RC filter of C_{SC}) accurately operates in Over−Current Protection operation (OCP).

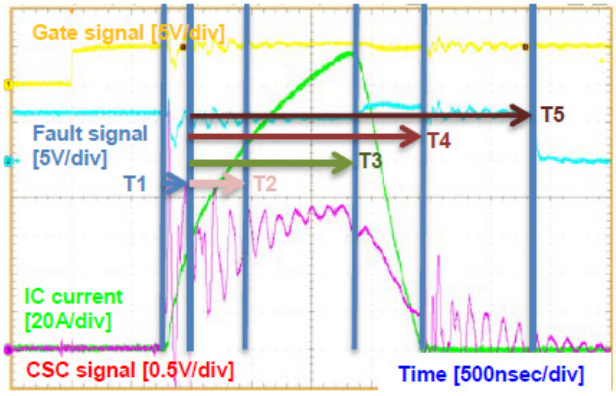


Figure 28. Short Circuit Waveform (NFVA33065L32, Ref. Condition: V_{DD} = 16.5 V, V_{DC} = 400 V, T_J = 25°C)

Table 14 shows actual real time at short circuit current protection. Each time sections have a distribution, so we have to consider of distribution.

Table 14. OVER−CURRENT (OC) PROTECTION TRIP LEVEL

Device	Typ. at T_J = 25°C	Typ. at T_J = 150°C	Max. at T_J = 25°C
NFVA33065L32	T2 = 0.80 μs	T2 = 0.52 μs	Considering ±20% distribution, T3 and T4
	T3 = 1.35 μs	T3 = 1.35 μs	
	T4 = 1.95 μs	T4 = 1.81 μs	
	T5 = 2.86 μs	T5 = 2.47 μs	

NOTES: To guarantee safe short−circuit protection under all operating conditions, CSC should be triggered within 1.0 μs after short−circuit occurs. (Recommendation: SCWT < 3.0 μs, Conditions: V_{PN} = 400 V, V_{DD} =16.5 V, T_J = 150°C).
It is recommended that delay from short−circuit to C_{SC} triggering should be minimized.

Fault Output Circuit

Because VFO terminal is an open−drain type; it should be pulled up via a pull−up resistor. The resistor must satisfy the above specifications.

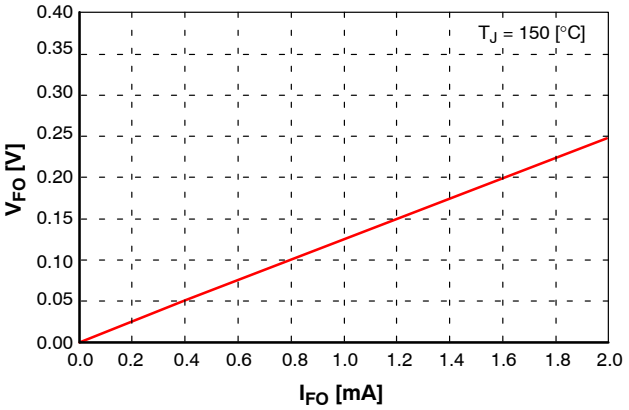


Figure 29. Voltage−Current Characteristics of V_{FO} Terminal

Bootstrap Circuit Design

Operation of bootstrap circuit

The V_{BS} voltage, which is the voltage difference between $V_{B(U,V,W)}$ and $V_{S(U,V,W)}$, provides the supply to the HVIC within the 650 V ASPM27 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high−side IGBT. The 650 V ASPM27 series includes an under−voltage lock out protection function for the V_{BS} to ensure that the HVIC does not drive the high−side IGBT, if the V_{BS} voltage drops below a specified voltage. This function prevents the IGBT from operating in a high dissipation mode. There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 30). This method has the advantage of being simples and inexpensive. However, the duty cycle and on−time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap to ground (either through the low−side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

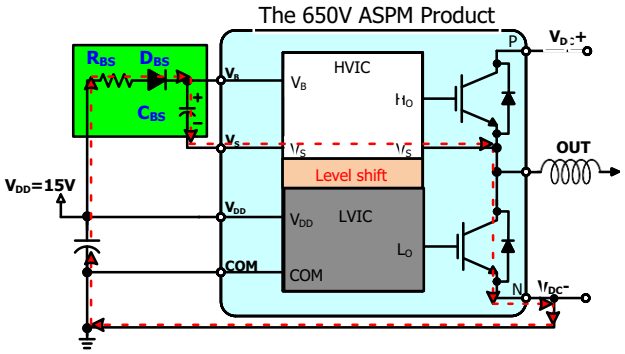


Figure 30. Current Path of Bootstrap Circuit

Selection of bootstrap capacitor considering initial charging

Adequate on−time of the low−side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\sigma} \times \ln \frac{V_{DD}}{V_{DD} - V_{BS(min)} - V_F - V_{LS}}$$

Where:
V_F = Forward voltage drop across the bootstrap diode
$V_{BS(min)}$ =The minimum value of the bootstrap voltage
V_{LS} = Voltage drop across the low−side IGBT or load
Δ = Duty ratio of PWM

When the bootstrap capacitor is charged initially; V_{DD} drop voltage is generated based on initial charging method, V_{DD} line SMPS output current, V_{DD} source capacitance, and bootstrap capacitance. If V_{DD} drop voltage reaches UV_{DD} level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, related parameter and initial charging method should be considered. To reduce V_{DD} voltage drop at initial charging, a large V_{DD} source capacitor and selection of optimized low−side turn−on method are recommended. Adequate on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts. Figure 31 to Figure 34 shows an example of initial bootstrap charging sequence. Once V_{DD} establishes, V_{BS} needs to be charged by turning on the low−side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency.

Therefore, it is desired to maintain this structure without creating complementary high−side PWM signals. The capacitance of V_{DD} should be sufficient to supply necessary charge to V_{BS} capacitance in all three phases. If a normal

PWM operation starts before V_{BS} reaches UVLO reset level, the high−side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over−current protection level.

Therefore, initial charging time for bootstrap capacitors should be separated that. The effect of the bootstrap capacitance factor and charging method (low−side IGBT driving method) is shown in Figure 31 and Figure 32.

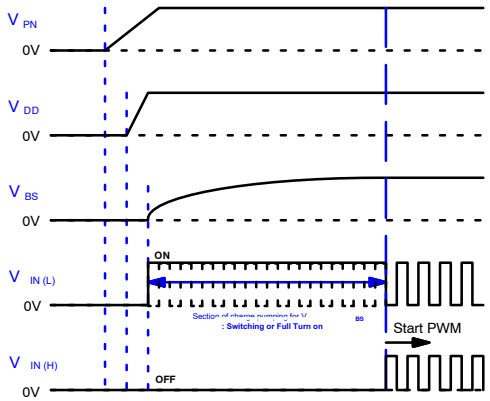


Figure 31. Timing Chart of Initial Bootstrap Charging

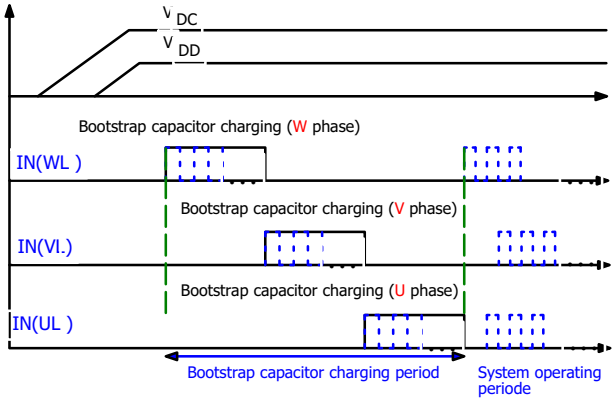


Figure 32. Recommended Initial Bootstrap Capacitors Charging Sequence

Figure 33 and Figure 34 shows waveform initial bootstrap capacitor charging voltage and current.

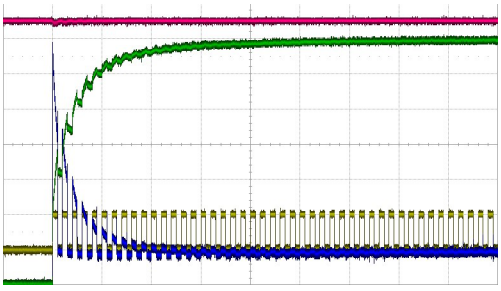


Figure 33. Each Part Initial Operating Waveform of Bootstrap Circuit (Conditions: V_{DC} = 300 V, V_{DD} = 15 V, C_{BS} = 22 μF, LS IGBT Turn−on Duty = 200 μsec)

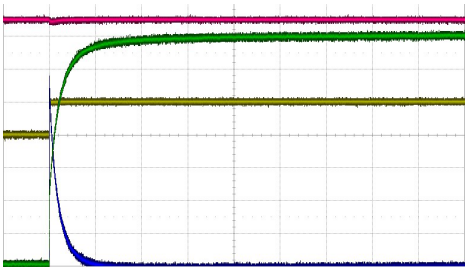


Figure 34. Each Part Operating Waveform of Bootstrap Circuit (Conditions: V_{DC} = 300 V, V_{DD} = 15 V, C_{BS} = 22 μF, LS IGBT Full Turn−on)

Selection of bootstrap capacitor considering operating

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}}$$

Where:

Δt: maximum on pulse width of high−side IGBT;

ΔV_{BS}: the allowable discharge voltage of the CBS (voltage ripple)

I_{leak}: maximum discharge current of the C_{BS}

Mainly via the following mechanisms:

- Gate charge for turning the high−side IGBT on.
- Quiescent current to the high−side circuit in HVIC.
- Level−shift charge required by level−shifters in HVIC.
- Leakage current in the bootstrap diode.
- C_{BS} capacitor leakage current (ignored for non−electrolytic capacitors).
- Bootstrap diode reverse recovery charge.

Practically, 4.4 mA of I_{Leak} is recommended for the 650 V ASPM27 series. By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The CBS is only charged when the high−side IGBT is off and the VS(x) voltage is pulled down to ground.

The on−time of the low−side IGBT must be sufficient to for the charge drawn from the CBS capacitor to be fully replenished. This creates an inherent minimum on−time of the low−side IGBT (or off−time of the high−side IGBT).

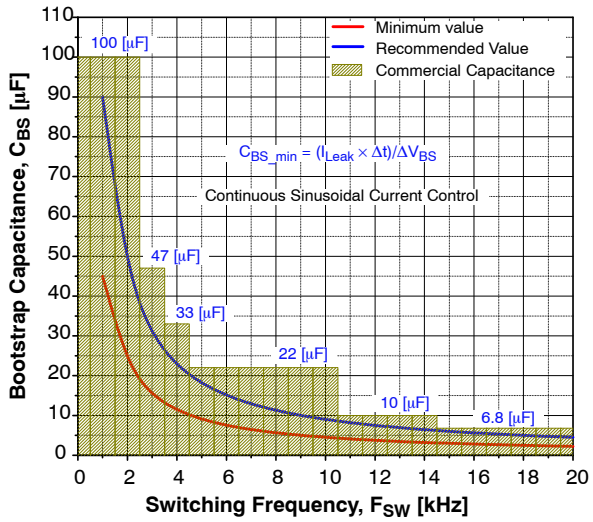


Figure 35. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔV_{BS}.

- I_{Leak}: circuit current = 4.4 mA (recommended value)
- ΔV_{BS}: discharged voltage = 0.1 V (recommended value)
- Δt: maximum on pulse width of high−side IGBT = 0.2 ms (depends on application)

$$C_{BS\_min} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} = \frac{4.4\ mA \times 0.2\ ms}{0.1\ V} = 8.8 \times 10^{-6}$$

→ More than 2 times → 18 μF

NOTE: The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended V_{BS} voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

Selection of a bootstrap diode

When the high−side IGBT or diode conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. Hence, a diode with withstand voltage of more than 650 V is recommended. It is important that this diode has a fast recovery (recovery time < 100 ns) characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the V_{DD} supply. The bootstrap resistor (R_{BS}) is to slow down the dV_{BS}/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.

Normally, a bootstrap circuit consists of bootstrap diode (D_{BS}), bootstrap resistor (R_{BS}), and bootstrap capacitor (C_{BS}).

The characteristics of the recommended bootstrap diode are:

- Fast recovery diode: 650 V/1.0 A
- trr: 80 ns (typical)
- Resistive characteristic: equivalent resistor of approximately 15 Ω

Selection of a bootstrap resistance

A resistor R_{BS} must be added in series with the bootstrap diode to slow down the dV_{BS}/dt and it also determines the time to charge the bootstrap capacitor. That is, if the minimum ON pulse width of low−side IGBT or the minimum OFF pulse width of high−side IGBT is t_O, the bootstrap capacitor has to be charged ΔV during this period. Therefore, the value of bootstrap resistance can be calculated by the following equation.

$$R_{BS} = \frac{(V_{CC} - V_{BS}) \times t_O}{C_{BS} \times \Delta V_{BS}}$$

Snubber Capacitor

Snubber Circuit

A snubber is an essential part of a power conversion circuit. Snubbers are used in power circuits for a broad array of applications including reducing or eliminating voltage or current spikes, limiting dV/dt, or dI/dt, reducing electromagnetic interference (EMI), reducing losses caused by switching operations, shaping load lines, and transferring power dissipation to resistors or useful loads.

A hard “switching” operation subjects a switch to voltage and current stress and causes high switching loss. Presence of parasitic capacitance and parasitic inductance increases this stress further. The total parasitic capacitance comprises of stray capacitance and junction capacitance while the total parasitic inductance comprises of lead inductance and inductance due to circuit layout. Using good circuit layout practices helps to minimize parasitic inductance.

Recommended wiring of shunt resistor and snubber capacitor

External current sensing resistors are applied to detect short−circuit or phase currents. A long wiring patterns between the shunt resistors and ASPM27 will cause excessive surges that might damage the 650V ASPM27s internal ICs and current detection components, and may also distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistors and ASPM27 should be as short as possible.

As shown in the Figure 36, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. If the snubber capacitor is installed in the wrong location ‘A‘ as shown in the Figure 36, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location ‘B‘, the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the SC protection level will be somewhat lower than the calculated design value. The “B” position surge suppression effect is greater than the location ‘A‘ or ‘C‘. The ‘C‘ position is a reasonable compromise with better suppression than in location ‘A‘ without impacting the current sensing signal accuracy. For this reason, the location ‘C‘ is generally used.

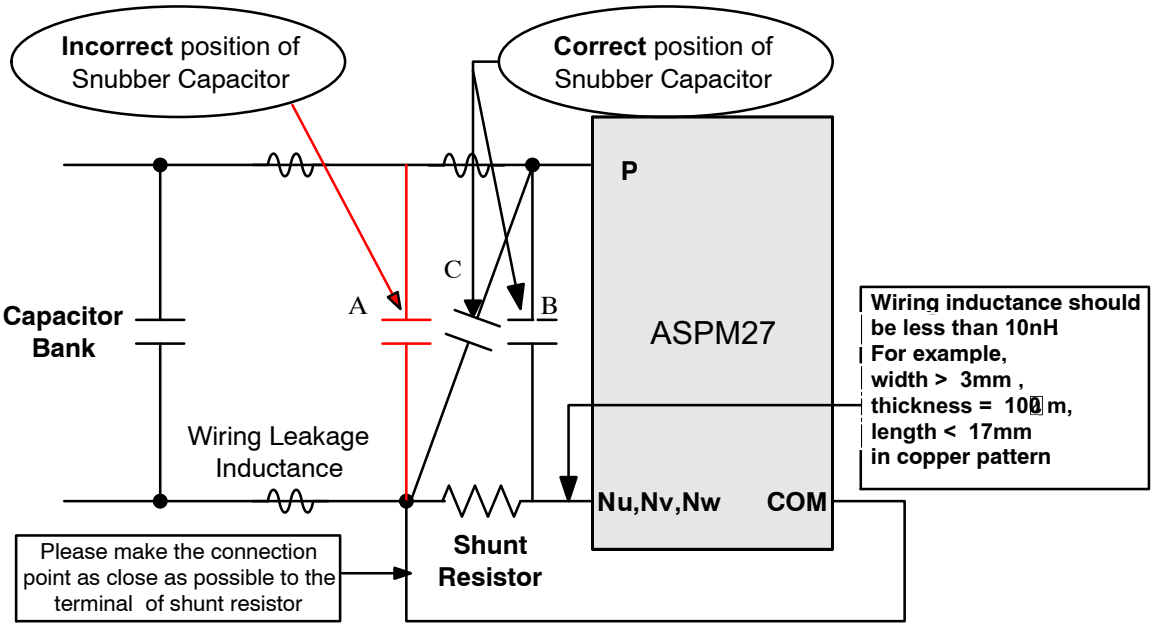


Figure 36. Recommended Wiring of Shunt Resistor and Snubber Capacitor

Snubber Capacitor Type

Snubber circuits are exposed to high stress, so it is important to select components that can withstand such conditions. The types of capacitors that are widely used for snubber applications include film and ceramic capacitors. Whereas plastic film capacitors can be used for both high power and low power circuits, ceramic capacitors are mostly used for low power applications.

Capacitors used in snubber circuits are subjected to high dV/dt and extremely high values of peak and rms current. These circuits demand capacitors that can withstand current spikes with high peak and rms values. The characteristics of polypropylene film capacitors make them suitable for snubber applications.

Film Capacitor

Most snubber capacitors are designed with polypropylene material. The performance characteristics of this low−loss dielectric material make it suitable for designing capacitors for use in both low and high pulse applications. The properties of a film capacitor are significantly dependent on the construction technology used.

Metallized film capacitors, also commonly known as metallized electrode capacitors, have self−healing properties while discrete foil electrode capacitors do not have them. Polypropylene film/foil capacitors are commonly used as snubber capacitors in low pulse applications.

Ceramic Capacitor

Multilayer ceramic (MLC) capacitors have many applications in today's electronic circuits.

Test Result

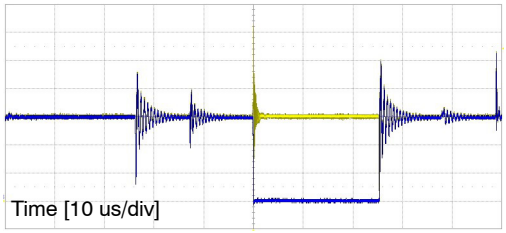
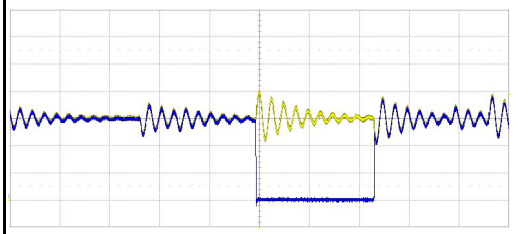
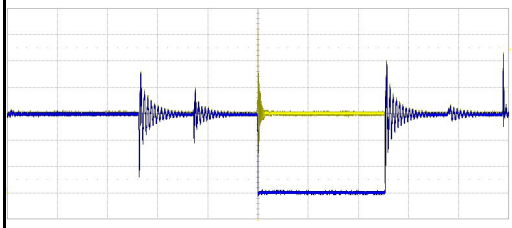
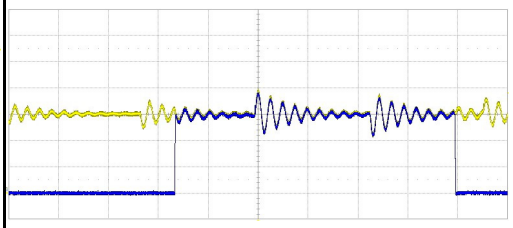
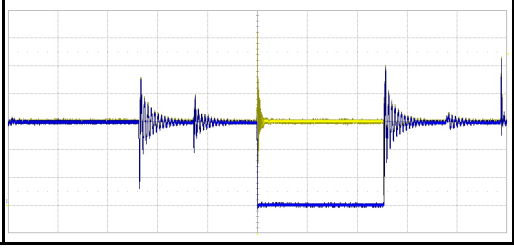
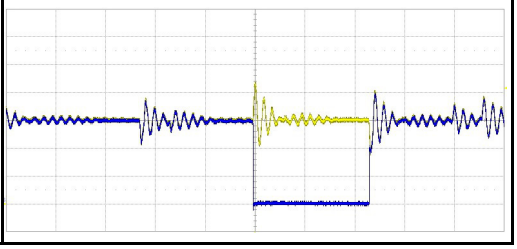
Generally, automotive application can't use polypropylene film capacitor because automotive application requires high temperature, also there is not enough space because it is a sealed structure inside the case as like E−comp, oil pump and etc.

Table 15 and Table 16 show the test results and waveforms by using the variable snubber capacitors. According to the test result, the box film capacitor show good performance in the below condition. However, customer have to find the good solution because of it is depend on the real operation condition and PCB layout. Test condition is V_{PN} = 300 V, V_{DD} = 15 V, Temp = room temp and wire length = 2 M wire from battery to ASPM27.

Table 15. TEST CONDITION AND RESULT

Snubber Type	Value	Surge Level	Maker	Remark
Without Snubber Capacitor	–	623 [V]	–	–
Box Film Capacitor 	0.1 uF	402 [V]	EPCOS/TDK 0.1 uF, 630 V	Surge level and capacitor temperature are lowest. If space is enough, it is best solution.
	0.2 uF	377 [V]		
	0.5 uF	354 [V]		
Polypropylene Film Capacitor 	0.1 uF	396 [V]	PILKOR 0.1 uF, 630 V	Surge level is lowest, but capacitor temperature is too high.
	0.2 uF	374 [V]		
	0.5 uF	354 [V]		
Ceramic Capacitor (MLC) 	0.1 uF	438 [V]	Murata 0.1 uF, 1000 V	Surge level is a little higher than another capacitor but no need space.
	0.2 uF	406 [V]		
	0.5 uF	377 [V]		

Table 16. WAVEFORM

Snubber Type	Without Snubber	With Snubber
Box Film Capacitor (0.1 uF)	CH1: VPN Voltage [100 V/div] CH2: Low−side IGBT V_{CE} voltage [100 V/div] 	
Polypropylene Film Capacitor (0.1 uF)		
Ceramic Capacitor (MLC) (0.1 uF)		

Circuit of Input Signal (IN(xH), IN(xL))

Figure 37 shows the I/O interface circuit between the MCU and ASPM27 product. Because the input logic is active HIGH and there are built−in pull−down resistors, external pull−down resistors are not needed.

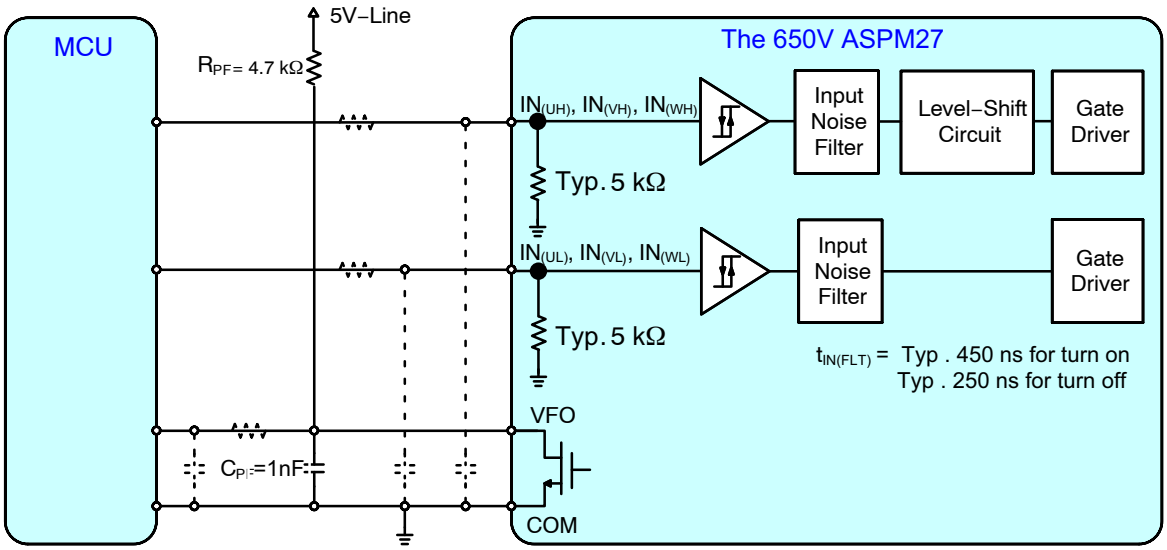


Figure 37. Recommended MCU I/O Interface CIrcuit

The input and fault−output maximum rated voltages are shown in Table 17. Since the fault−output is open drain, its rating is V_{CC} + 0.3 V, and 15 V supply interface is possible. However, it is recommended that the fault output be configured with the same supplies as the input signals. It is also recommended that the de−coupling capacitors be placed at both the MCU and ASPM27 ends of the V_{FO} signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 37) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of ASPM27 integrates a 5 kΩ (typical) pull−down resistor. Therefore, when using an external filtering resistor between the MCU output and the module series input, attention should be given to the signal voltage drop at the module input terminals to satisfy the turn−on threshold voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown dotted in Figure 37.

Table 17. MAXIMUM RATINGS OF INPUT AND VFO PINS

Symbol	Item	Condition	Rating	Unit
V_{IN}	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$ − COM (x)	−0.3~Vcc + 0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} − COM (L)	−0.3~Vcc + 0.3	V

Table 18. INPUT THRESHOLD VOLTAGE RATINGS (V_{CC} = 15 V, T_J = 25°C)

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
$V_{IN(ON)}$	Turn−On Threshold Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ − COM (H)		1.8	2.6	V
$V_{IN(OFF)}$	Fault Output Supply Voltage	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ − COM (L)	0.8	1.7		V

PRINT CIRCUIT BOARD (PCB) DESIGN

General Application Circuit Example

Figure 38 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 39 shows guidance of PCB layout for the 650 V ASPM27series.

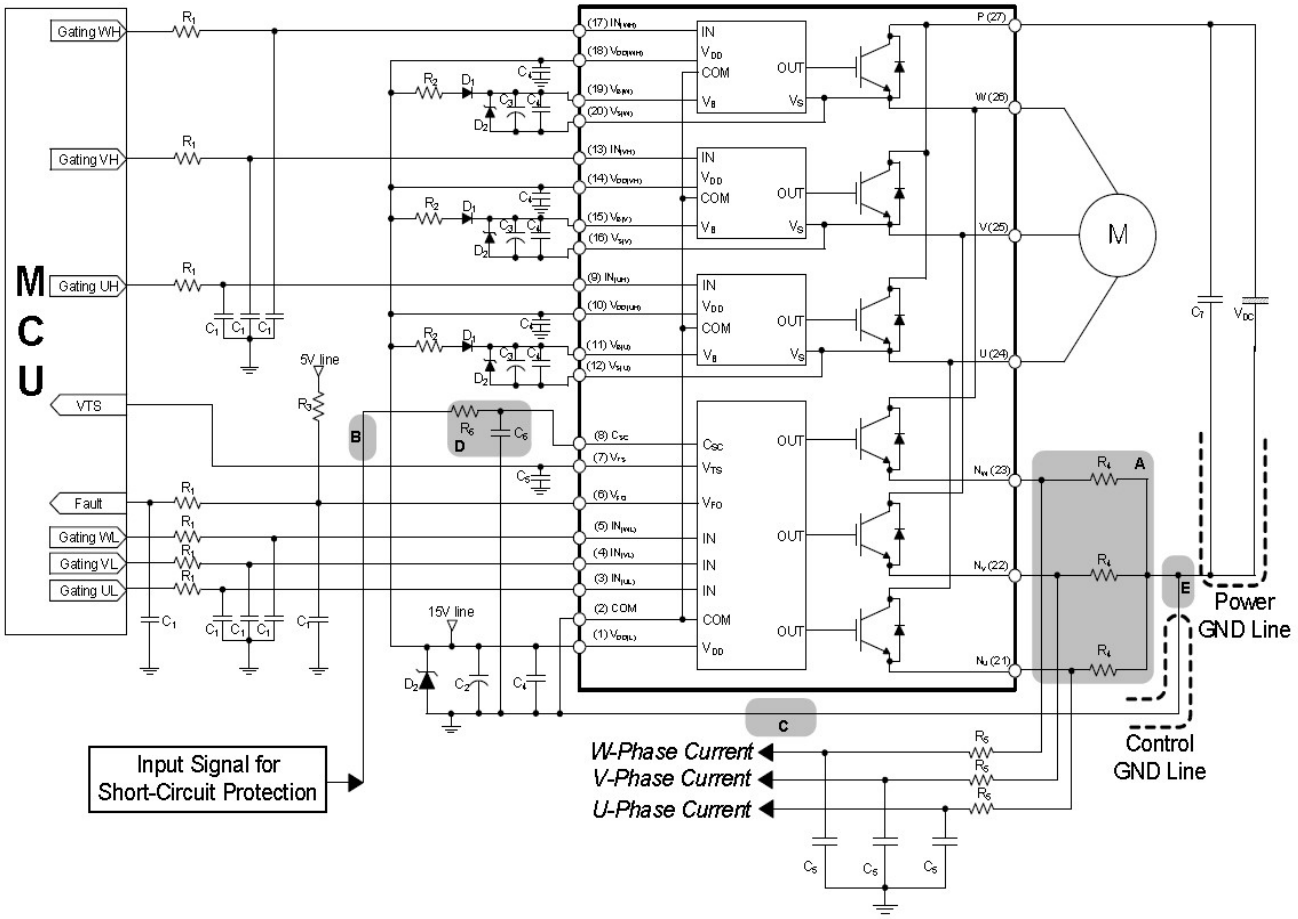


Figure 38. General Application Circuity for the 650 V ASPM27 Series

PCB Layout Guidance

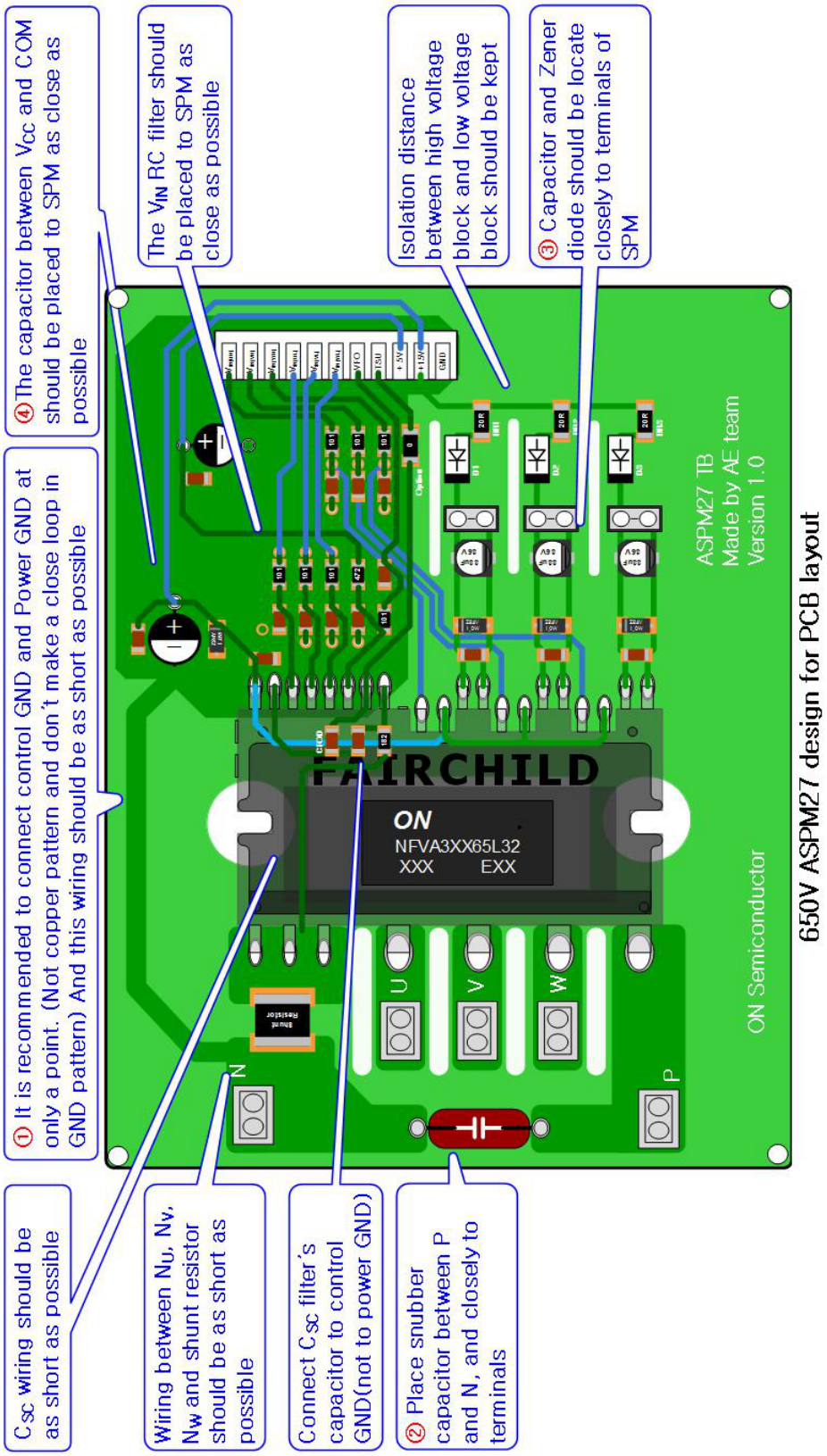
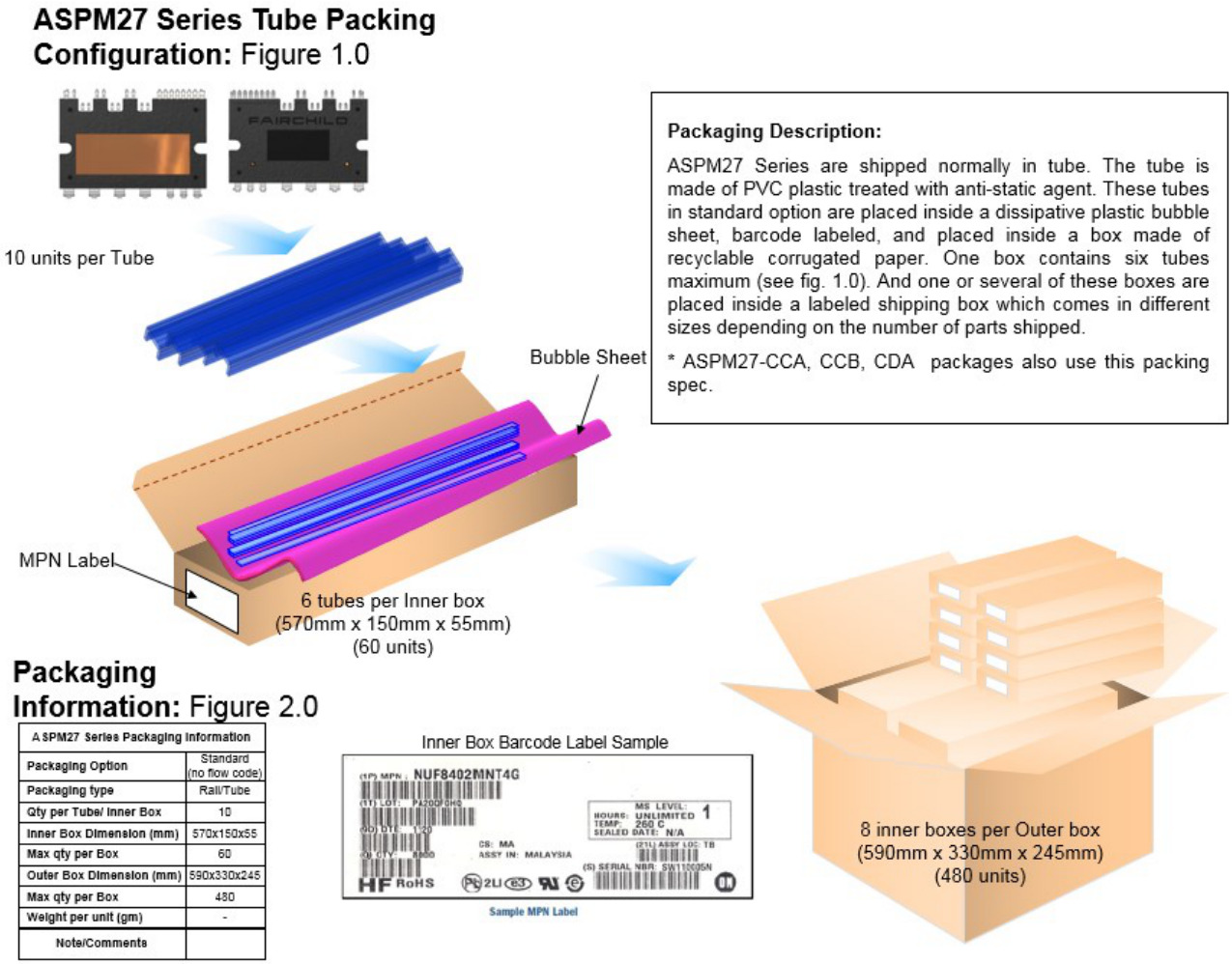


Figure 39. Print Circuity Board (PCB) Layout Guidance for the 650 V ASPM27

PACKING INFORMATION



Packaging Information: Figure 2.0

ASPM27 Series Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	10
Inner Box Dimension (mm)	570x150x55
Max qty per Box	60
Outer Box Dimension (mm)	590x330x245
Max qty per Box	480
Weight per unit (gm)	-
Note/Comments	

Tube Information : Figure 3.0

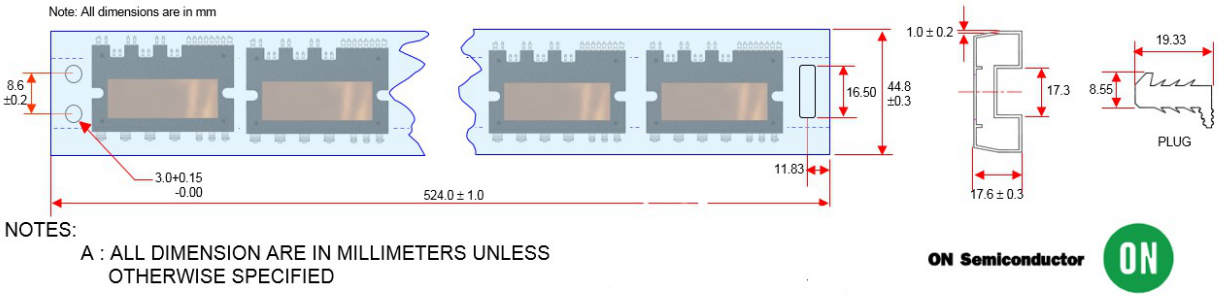


Figure 40. Packing Information

RELATED RESOURCES

- FAM65V05DF1 Product Folder
- NFVA33065L32, NFVA34065L32, NFVA35065L65 Product Folder
- AN−9086 − 600V SPM® 3 Series Mounting Guidance

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